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256-ELEMENT SCHOTTKY-BARRIER IR-CCD LINE SENSOR.(U)

SEP 77 W F KOSONOCKY, D J SAUER

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## 256-ELEMENT SCHOTTKY-BARRIER IR-CCD LINE SENSOR

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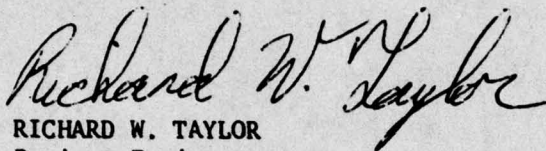
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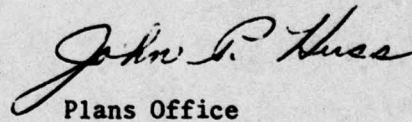
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output registers. At 77 K the buried-channel CCD output registers had a measured charge-transfer loss of  $5 \times 10^{-5}$  per transfer. The Schottky-barrier detectors are designed for operation in a continuous-charge-skimming mode that results in a very low leakage current density which was measured as  $1.4 \times 10^{-9}$  A/cm<sup>2</sup> at 77 K. The quantum efficiency coefficient  $C_1$  of the platinum silicide Schottky-barrier detectors was estimated to be 0.1, and detector-to-detector response uniformity of 8% maximum peak-to-peak, or about 1.2% rms, was measured.

1400 microAmp/sq cm.

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## EVALUATION

This report is the Final Report on the contract. This effort demonstrated the feasibility of monolithically integrating infrared detectors with CCD readouts. Specifically, a line array of 256 platinum silicide Schottky barrier infrared detectors was integrated with two double-polysilicon-gate buried channel CCD's on one substrate. These devices will be used as sensors for a passive infrared radiometric fence security system. This work was performed in support of the Base and Installation Security System (BISS) program to develop sensors for physical security systems.

*Richard W. Taylor*  
RICHARD W. TAYLOR  
Project Engineer

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## PREFACE

This Final Report was prepared by RCA Laboratories, Princeton, New Jersey, under Contract No. F19628-76-C-0254. It describes work performed from June 1, 1976 to March 31, 1977, in the Integrated Circuit Technology Center, J. H. Scott, Director. The Project Supervisor was K. H. Zaininger, and the Principal Investigator is W. F. Kosonocky. Other Members of the Technical Staff who participated in this program were J. Banfield, D. J. Sauer, and F. V. Shallcross. The coding of the chip layout was done by G. M. Meray; the devices were processed by L. M. Bijaczyk, W. S. Romito, and R. Miller; the waveform generator was constructed by C. Y. Tayag, and R. A. Criado participated in the device and wafer testing.

The manuscript of this report was submitted by the authors on June 30, 1977. Publication of this report does not constitute Air Force approval of the report's findings or conclusions. It is published only for exchange and stimulation of ideas.

The Air Force Technical Monitor is R. W. Taylor.

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## SECTION I

### INTRODUCTION

The feasibility of high resolution thermal imaging by the use of platinum silicide Schottky-barrier Infrared Charge-Coupled Devices (IR-CCDs), as well as the potential performance of such a system, was demonstrated with devices developed at RCA Laboratories, Princeton, New Jersey, (under Contract No. F19628-73-C-0282, supported by ARPA, and monitored by RADC/ET) and measured at RADC/ET [1,2]. The first-generation platinum silicide Schottky-barrier IR-CCD was a 64-element device made with a single-metal surface-channel charge-coupled readout register. The 256-element device made with double-polysilicon overlapping-gate buried-channel CCD readout developed under this contract represents the second generation of such IR-CCDs. This device was developed for the DOD-BISS Program Office to be used as an active element for a radio-metric fence line sensor.

Platinum silicide on p-type silicon has a barrier height of 0.27 eV, corresponding to a cutoff wavelength of 4.5  $\mu\text{m}$ . The effective quantum efficiency for thermal imaging of platinum silicide Schottky-barrier detectors is rather small, on the order of 0.1%. However, the demonstrated high uniformity of photoresponse (0.5% rms and better) [1-3] combined with low noise readout by buried-channel CCDs make the Schottky-barrier IR-CCDs attractive alternatives for many thermal imaging applications. The rather low quantum yield in Schottky detectors can be made-up by operating the arrays either in the staring or time-delay-integration mode. Calculations [1,2] based on present estimates indicate that these devices should be capable of resolving 0.1°C targets against a 300 K background at standard video frame rates.

1. F. D. Shepherd, et al., "Ambient Thermal Response of a Monolithic Schottky IR-CCD," Proc. of the IRIS Thermal Imaging Specialty Group Meeting, El Toro, CA, Feb. 1977.
2. R. W. Taylor, et al., "Schottky IR-CCDs," Proc. IRIS Detector Specialty Group Meeting, 22-24 March 1977, Air Force Academy, Colorado Springs, CO.
3. E. S. Kohn, W. F. Kosonocky, and F. V. Shallcross "Charge-Coupled Scanned IR Imaging Sensors," Final Report, Contract No. F19628-73-C-0282 (to be published).

## SECTION II

### DESCRIPTION OF THE ARRAY

#### A. GENERAL SYSTEM

The system block diagram of the platinum silicide Schottky-barrier infrared line sensor with charge-coupled readout (designated TC 1204) developed under this contract is illustrated in Fig. 1. This IR-CCD line sensor has an array of 256 Schottky-barrier detectors designed with 5 to 1 aspect ratio. The detectors are about 8 mil long, and are positioned on 1.6-mil centers. The array of Schottky-barrier detectors is read out by the Output Register A. Output Register B has common clock electrodes with Output Register A. The output registers have been designed also with identical input and output circuits. The dual output-register construction is intended here to be used with differential output sensing for clock pickup cancellation. Furthermore, when the output of Register A is fed into the input of Register B, the differential output sensing can be used for MTI operation, or the device can be operated in the background subtraction mode.

#### B. CHIP LAYOUT

The chip layout of the 256-element Schottky-barrier IR-CCD is illustrated in Figs. 2 to 5. In Fig. 2 photomicrographs of the input and output sections of the array are shown. All of the electrical terminals in this figure are labeled, with the exception of the substrate connection (SUB) which is shown later in the photographs of the complete 30-pin package in Figs. 11 and 12. The 256-element IR-CCD is contained on a 444 x 68 mil chip.

##### 1. Schottky-Barrier Detectors

The photomicrograph in Fig. 3 shows the construction of the platinum silicide Schottky-barrier infrared detectors in more detail. These detectors are positioned on 1.6-mil centers and, as shown in the layout sketch in Fig. 4, the nominal active area of each detector is 7.8 x 0.5 mil. Each platinum silicide detector is surrounded by an implanted n-type guard ring, however, and there is also an  $n^+$ -diffusion which connects the Schottky diode with the

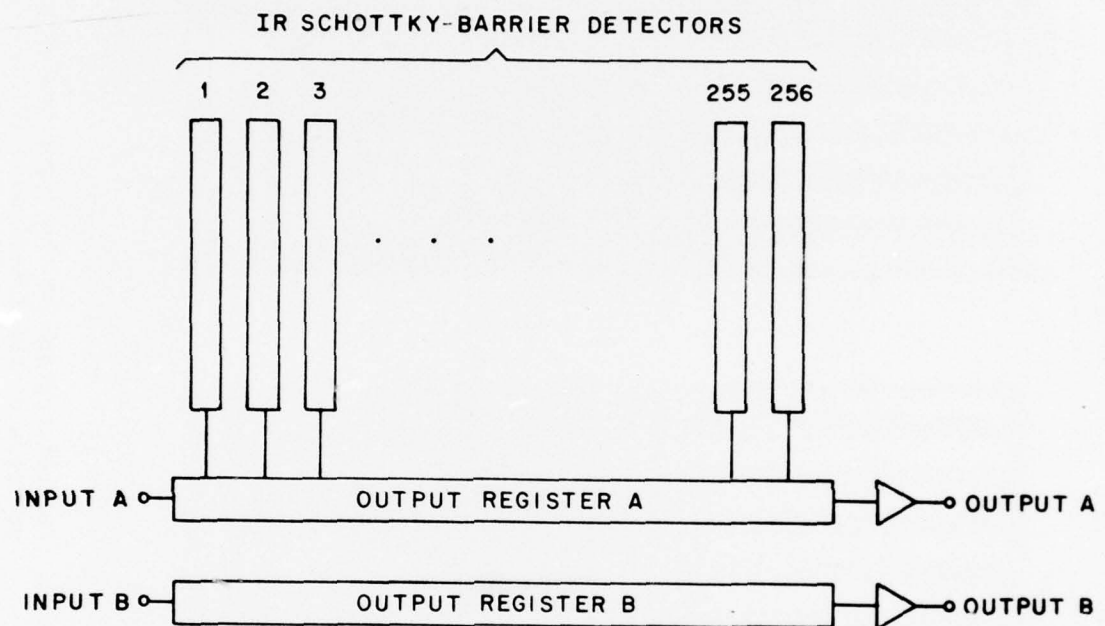


Figure 1. Block diagram of 256-element IR-CDD.

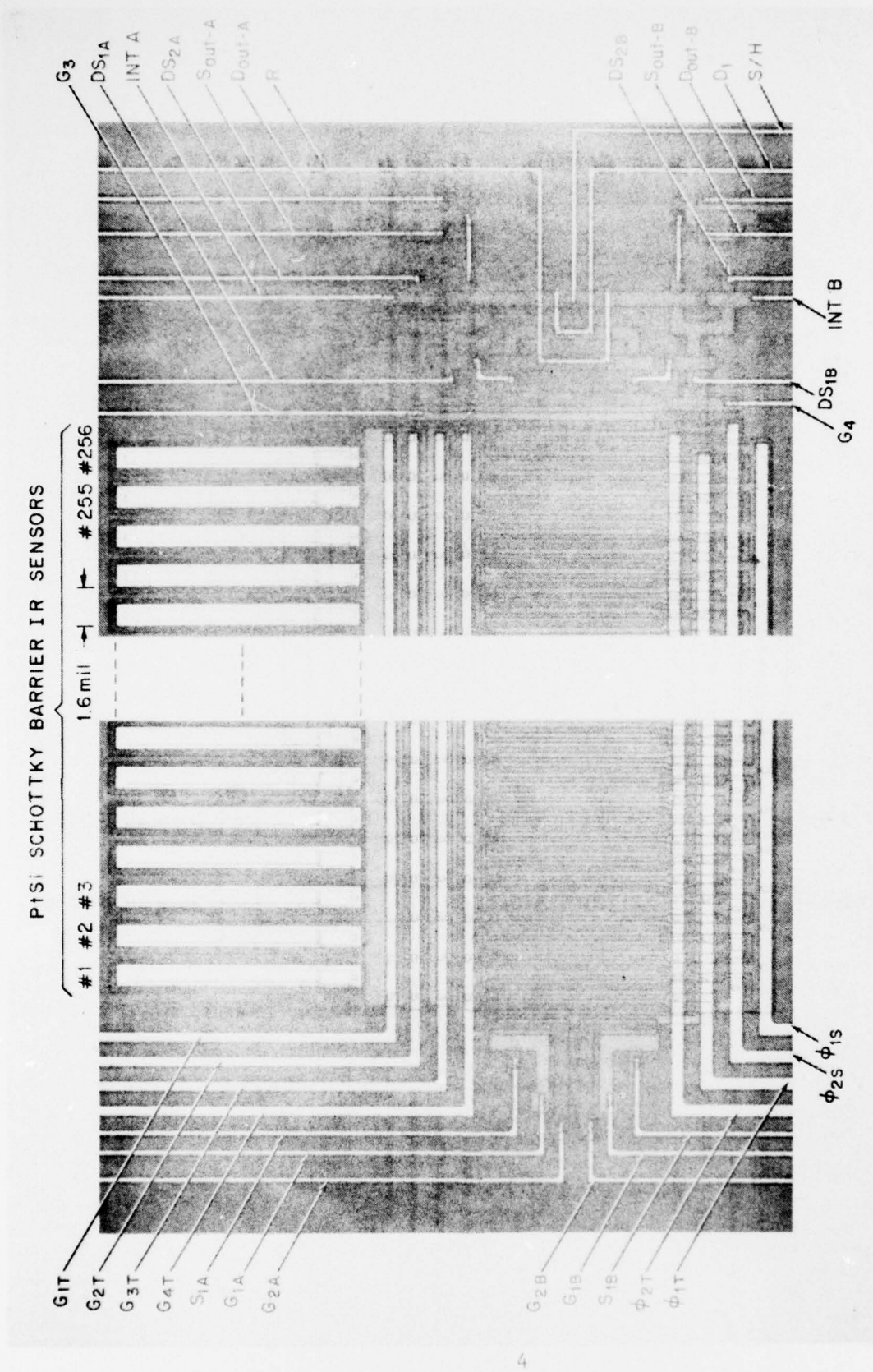


Figure 2. Photomicrograph of the input and output sections of the 256-element IR-CCD.

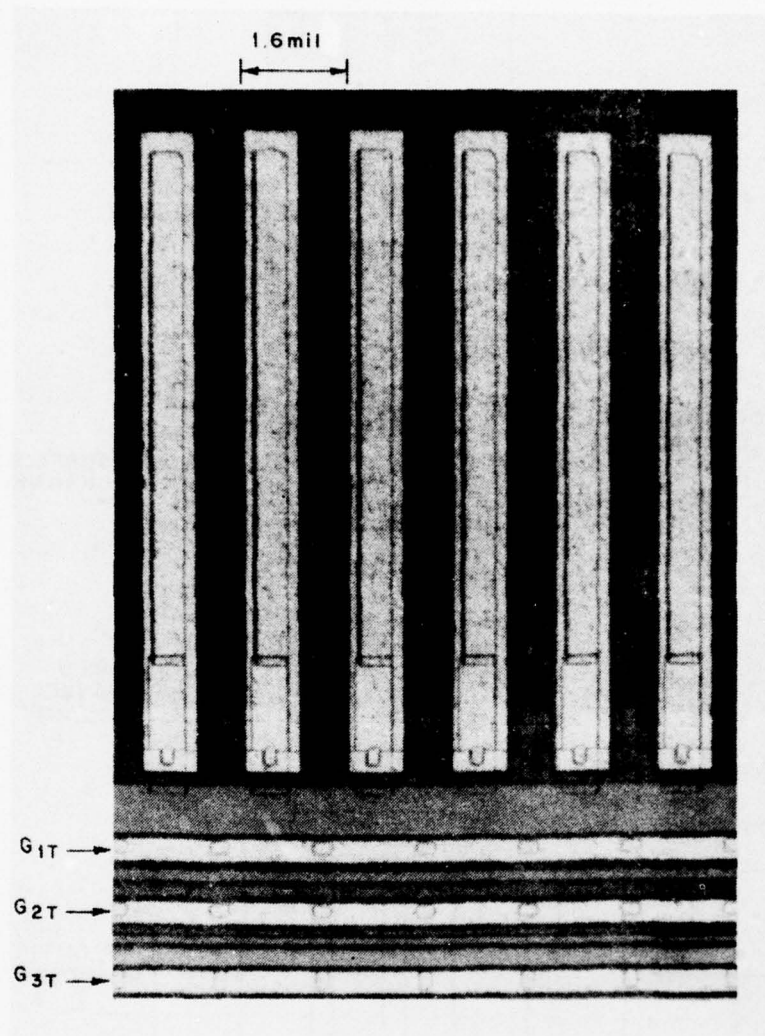


Figure 3. Photomicrograph of the platinum silicide Schottky-barrier detectors.

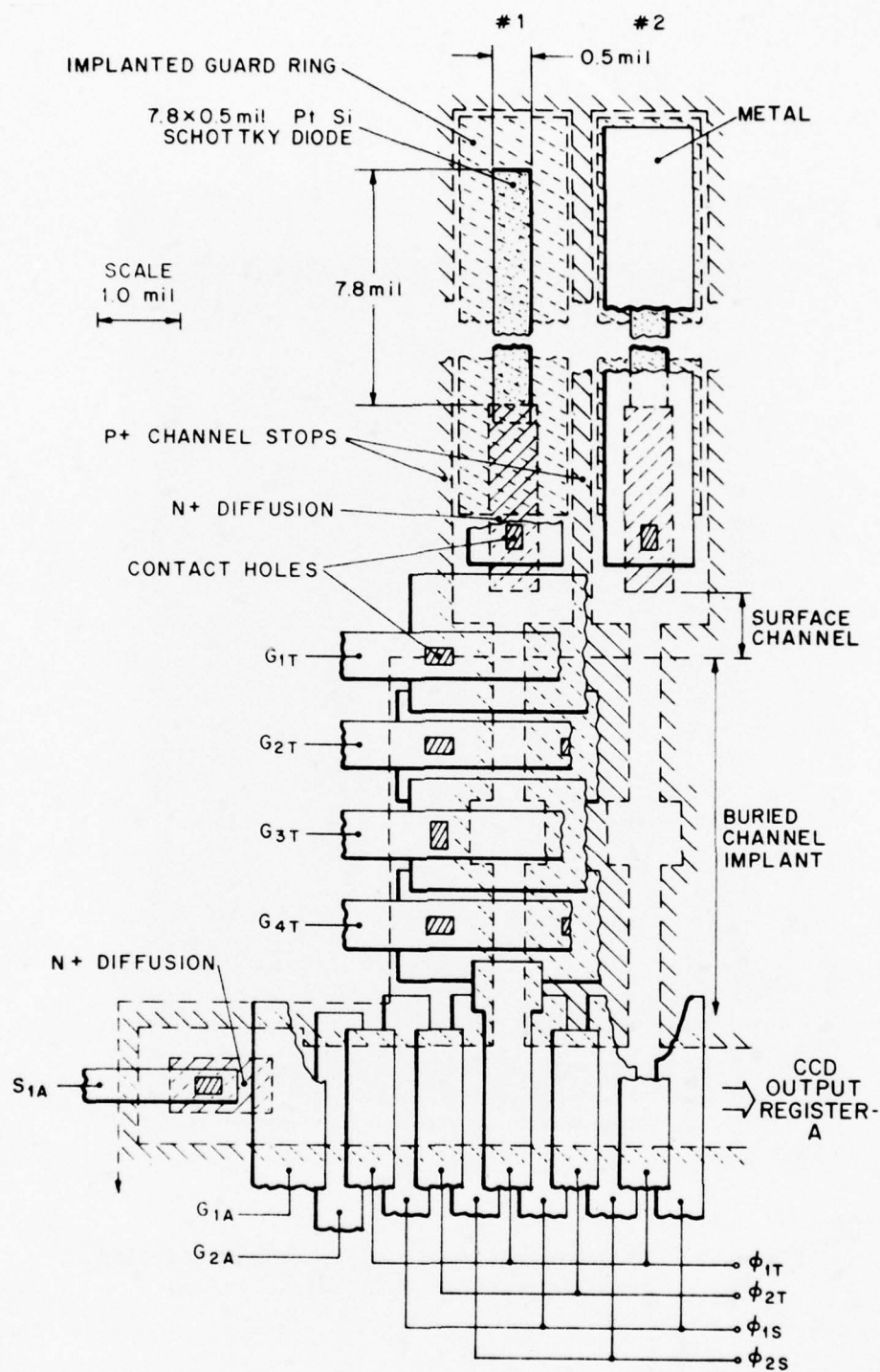


Figure 4. Detailed layout of the Schottky-barrier detectors, charge integration CCD stages (Gates G<sub>1T</sub>, G<sub>2T</sub>, and G<sub>3T</sub>, and the input part of Output Register A.

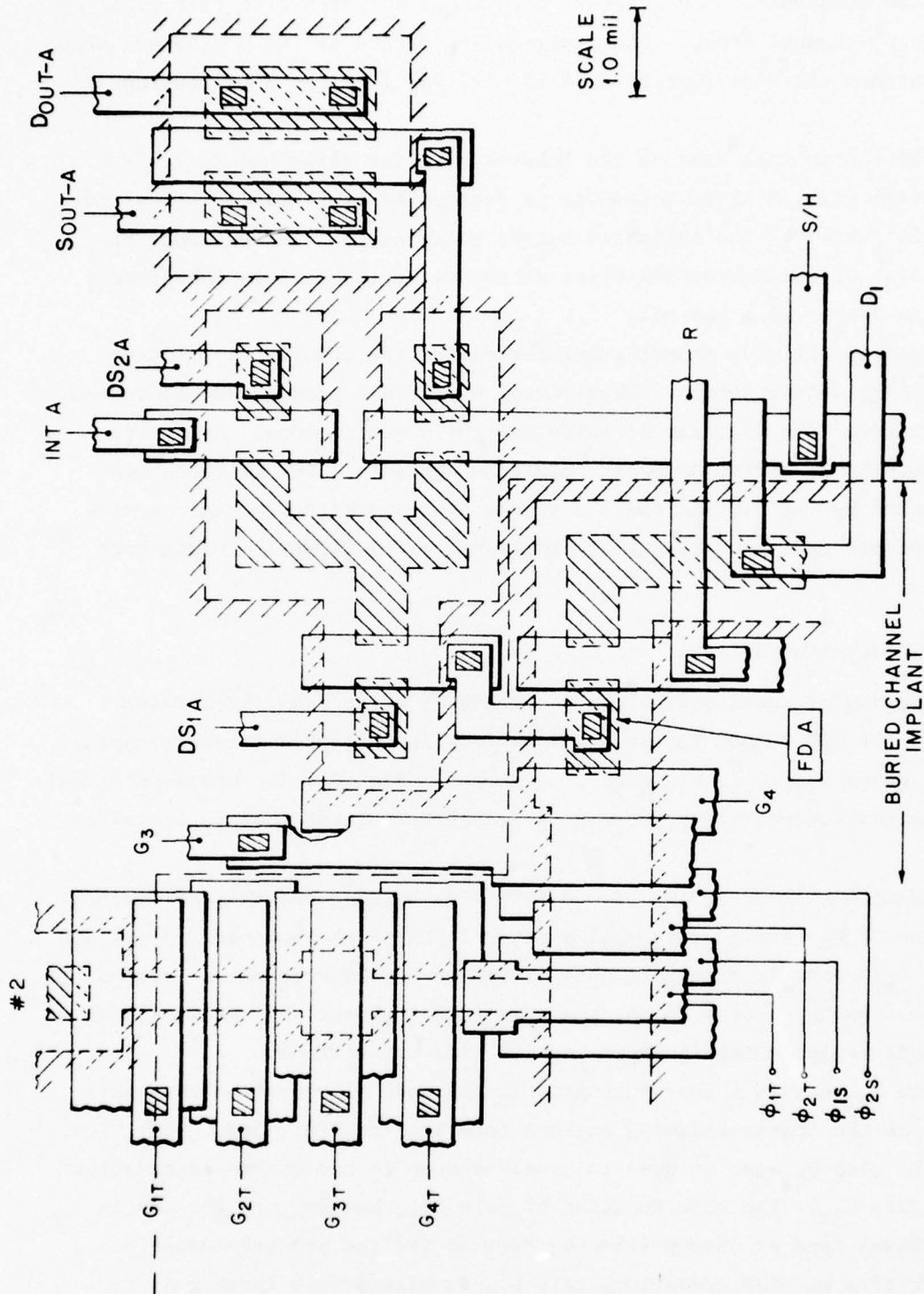


Figure 5. Detailed layout of the output section of Output Register A.

charge-coupled structure. The Schottky diodes are isolated from each other by 0.2-mil-wide  $p^+$ -channel stops. The designed separation of the  $p^+$ -channel stops from the platinum silicide regions is 0.45 mil, and from the  $n^+$ -diffusions is 0.4 mil.

Although the nominal size of the Schottky-barrier detectors is  $7.8 \times 0.5$  mil, the actual size of these detectors is reduced by mask misalignments and by lateral diffusion of the implanted n-type guard rings. Our estimate of the actual size of the Schottky-barrier detectors in the devices fabricated and tested is about  $7.7 \times 0.4$  mil.

The platinum silicide Schottky-barrier diodes are covered by titanium aluminum (Ti-Al) metallization. These metal electrodes provide an electrical connection between the platinum silicide and the  $n^+$ -diffusions. Actually, this is accomplished by two somewhat redundant contacts. One of these contacts is formed by the 0.2-mil overlap of the platinum silicide regions with the  $n^+$ -diffusions and the other by an additional  $0.2 \times 0.2$ -mil contact hole shown below.

## 2. Charge-Integration Stages

The coupling of the detected charge signal from the Schottky-barrier detectors to the CCD Output Register A is accomplished by the metal-strapped polysilicon gates  $G_{1T}$ ,  $G_{2T}$ ,  $G_{3T}$ , and  $G_{4T}$ , shown in Fig. 4. The cross-sectional view of this charge-coupling structure is illustrated later (not to scale) in Fig. 9.

The function of the gate  $G_{1T}$  is to form a dc barrier between the Schottky diode and the charge integration well under gate  $G_{3T}$ . As shown in Figs. 4 and 9, the gate  $G_{1T}$  controls a surface channel region adjacent to the  $n^+$ -region touching the Schottky diode. Also, the same gate  $G_{1T}$  overlaps the implanted buried-channel region extending into the CCD readout sections.

The gate  $G_{2T}$  serves a dual purpose. In the mode of operation when gate  $G_{1T}$  is used as the charge-skimming barrier (see Section IID., Figs. 9(b), (c), and (d)), the gate  $G_{2T}$  can be used to couple charge to the charge integration well under gate  $G_{3T}$ . The main function of gate  $G_{2T}$ , however, is for use as a buried-channel type of charge-skimming barrier for the Schottky-diode detectors. In this mode of operation, gate  $G_{1T}$  is biased with large positive dc voltage, thus effectively extending the diffusion region in contact with the Schottky diodes [see Fig. 9(e)].

Finally, the function of the gate  $G_{4T}$  is to isolate the charge integration wells under the gate  $G_{3T}$  from the CCD Output Register A. As shown in Figs. 4 and 5, the charge-coupling from the charge-integration wells under gate  $G_{3T}$  to Output Register A is accomplished via gate  $G_{4T}$  and clock gates  $\phi_{1T}$ . Since the output registers are designed to operate as 2-phase CCD's, the use of the transfer gates ( $\phi_{1T}$ ) rather than the storage gates ( $\phi_{1S}$ ) for coupling of the charge signals into the output register should minimize the charge-transfer loss resulting from the widening of the output register channel in these regions.

### 3. Dual CCD Output Registers

The input and output sections of the dual CCD output registers are shown on the photograph in Fig. 2, and more detailed (to scale) layouts are given in Fig. 4 and 5 for Output Register A. Output Register B is identical to Output Register A with the exception of the wider channel regions under the  $\phi_{1T}$  electrodes. Both output registers are buried-channel, 1.2 mil wide, defined by  $p^+$ -channel stops, and powered by common clock electrodes. The output registers have also been designed with identical input and output structures that should be insensitive to mask alignment variations. Special attention was given to the design of the output amplifiers to assure symmetrical clock pickup in the two output channels (see Fig. 5 for details).

The charge-coupling structure between the Schottky-barrier detectors and the output registers, as well as the dual output registers, have been designed for construction with double-polysilicon overlapping-gate sealed-channel construction. Since this device is made on a rather large chip (444 x 68 mil) all of the gates were designed with 0.2-mil overlaps. The nominal sizes of all the gates are shown to scale in Fig. 4 and 5. The output registers are designed with 1.6-mil stages. Each polysilicon level has 0.6-mil gates with 0.2-mil spaces. Thus, the effective length of the storage gates is 0.6 mil and of the transfer gates 0.2 mil.

The output registers were designed for operation with the charge-preset (fill and spill) inputs (See Fig. 6). When operated with the waveform generator described in Section III, the source diffusions  $S_{1A}$  and  $S_{1B}$  have a common electrical input  $V_{S1}$ , and the input gates  $G_{1A}$  and  $G_{1B}$  have a common input  $V_{G1}$ .

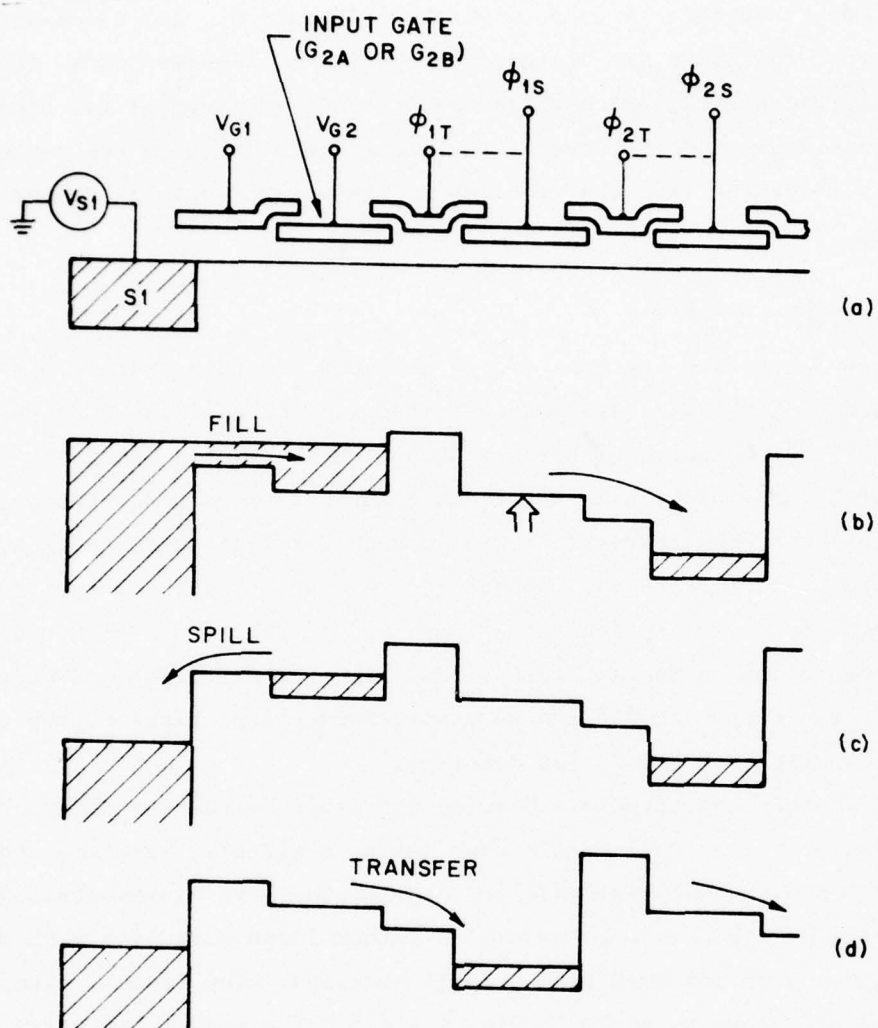


Figure 6. Construction and operation of the charge-preset input structure of the output registers.

The charge inputs are adjusted to the desired values in the two output registers by two separate input signals  $V_{G2A}$  and  $V_{G2B}$ .

The construction of the output end of the dual output registers is illustrated in Figs. 5 and 7(a). Here, the floating diffusions, FD-A and FD-B, are periodically reset to the drain D-1 by a common reset gate R, as shown in Figs. 7(b) and (c). The charge signals are coupled into the respective floating diffusions, FD-A and FD-B, from the dual registers by common gates G3 and G4. The gate G3 is powered by the clock phase  $\phi_{1T}$ , and gate G4 is dc biased to provide isolation between the clock-phase  $\phi_{1T}$  and the floating diffusions FD-A and FD-B.

#### 4. Output Amplifiers

The signal output detected by the floating diffusions FD-A and FD-B are amplified by two identical output amplifiers illustrated in Fig. 8. The scaled layout of one of these amplifiers has been shown in Fig. 5. All the MOS devices are designed for first-level polysilicon gates with channel length of 0.4 mil (defined by the source to drain spaces of the mask) and the effective channel width indicated in Fig. 8.

The output amplifier has been originally designed for operation in several modes. The first amplifier stage consisting of MOS devices  $Q_3$  and  $Q_5$  or  $Q_4$  and  $Q_6$  could be operated as an inverter or as a source follower. In the inverter (integration) mode the load devices  $Q_5$  or  $Q_6$  could be used as periodically resettable switches. The integration mode of operation, however, did not prove to have any appreciable advantages over the source-follower operation of the first stage of the output amplifier.

The MOS devices  $Q_7$  and  $Q_8$  provide the option of operating the amplifier either in the direct-coupling mode or a sample-and-hold mode. (Again, the operation in the direct-coupling mode turned out to be less noisy). The output MOS devices  $Q_9$  and  $Q_{10}$  were designed to be wide enough to provide low output impedance for off-the-chip signal coupling.

#### C. TECHNOLOGY

The charge-coupling structure of this array is constructed with an overlapping-gate, double-polysilicon, CCD technology developed at RCA Laboratories

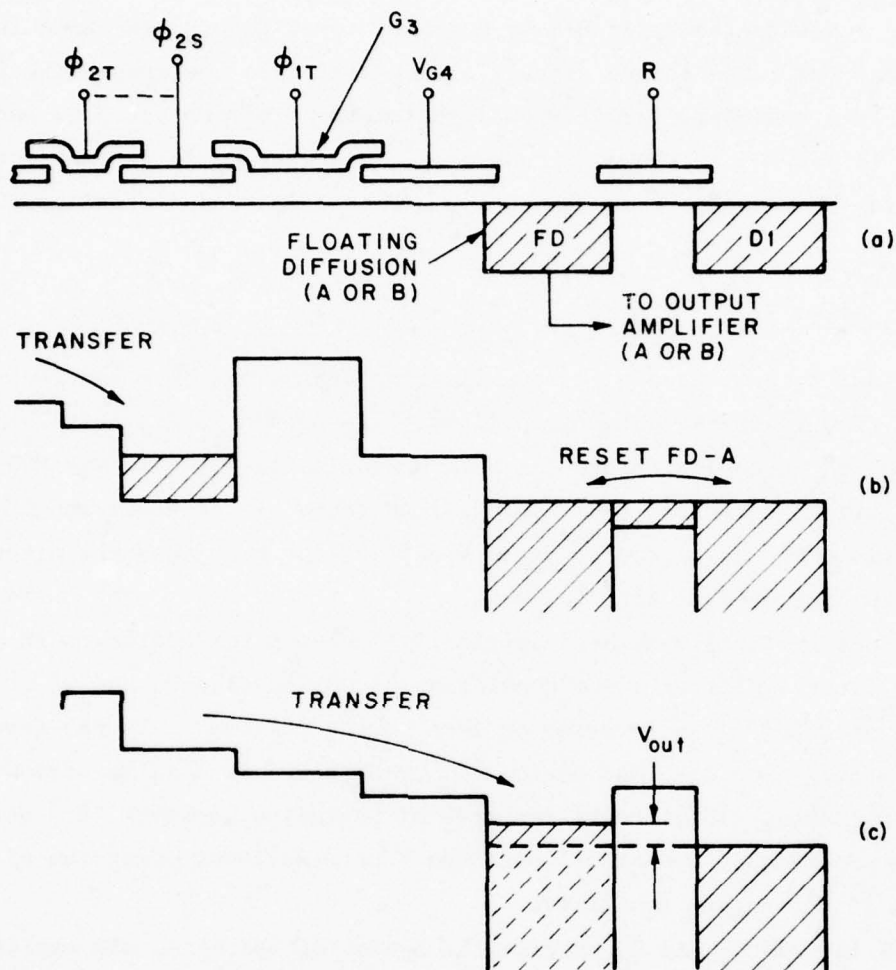


Figure 7. Construction and operation of the floating diffusion periodically reset to drain-diffusion potential of the output registers.

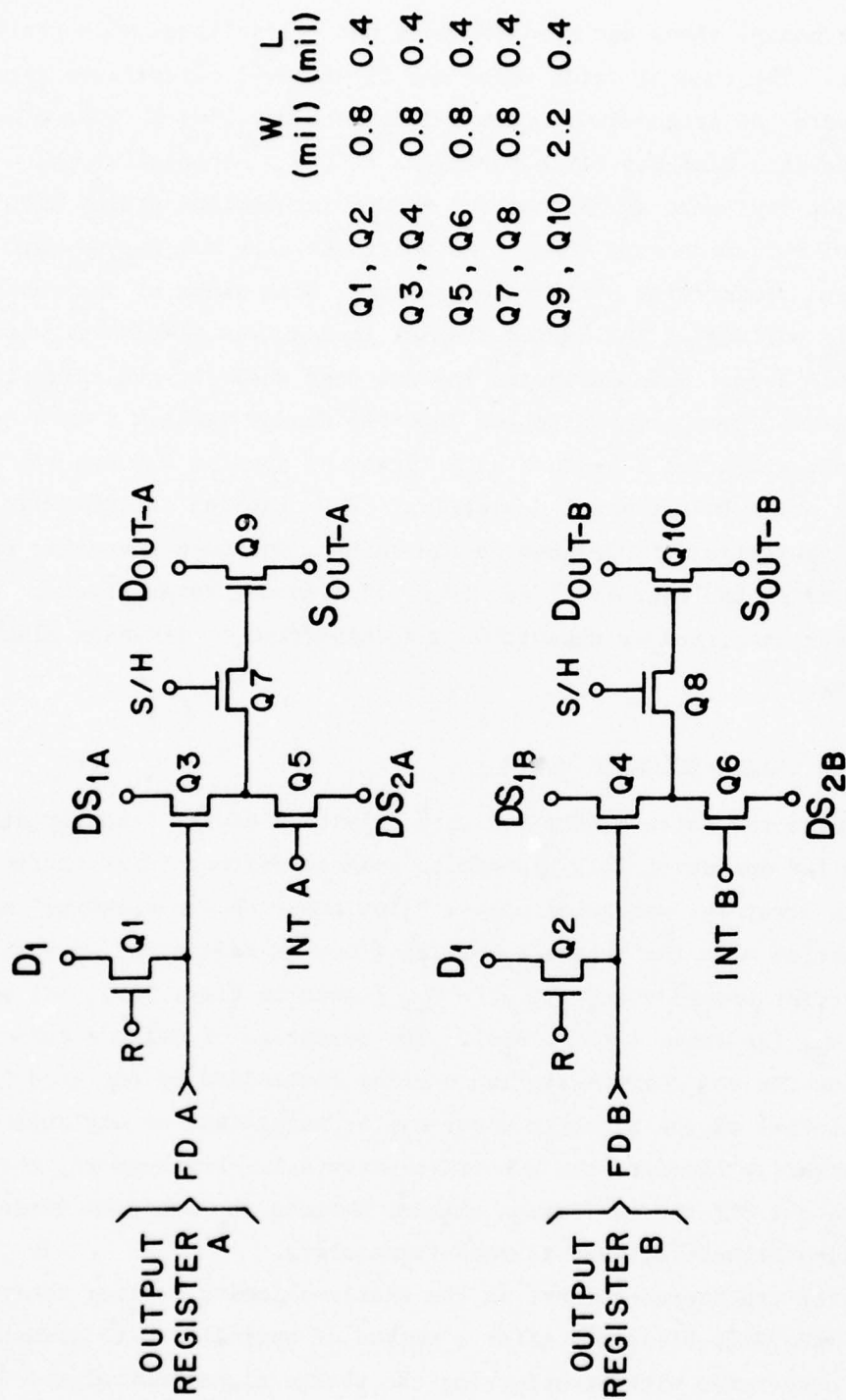


Figure 8. Circuit diagram of the dual-output amplifiers.

Princeton, N. J. The devices constructed and tested under this contract were made with  $p^+$ -channel stops and  $n^+$ -diffusions not self-aligned with the polysilicon gates. The channel oxide under the first-level polysilicon gate was 1400 Å and under the second-level polysilicon gate was 2500 Å. The  $n^+$ -diffusions were designed with 0.4-mil separations to the  $p^+$ -channel stops.

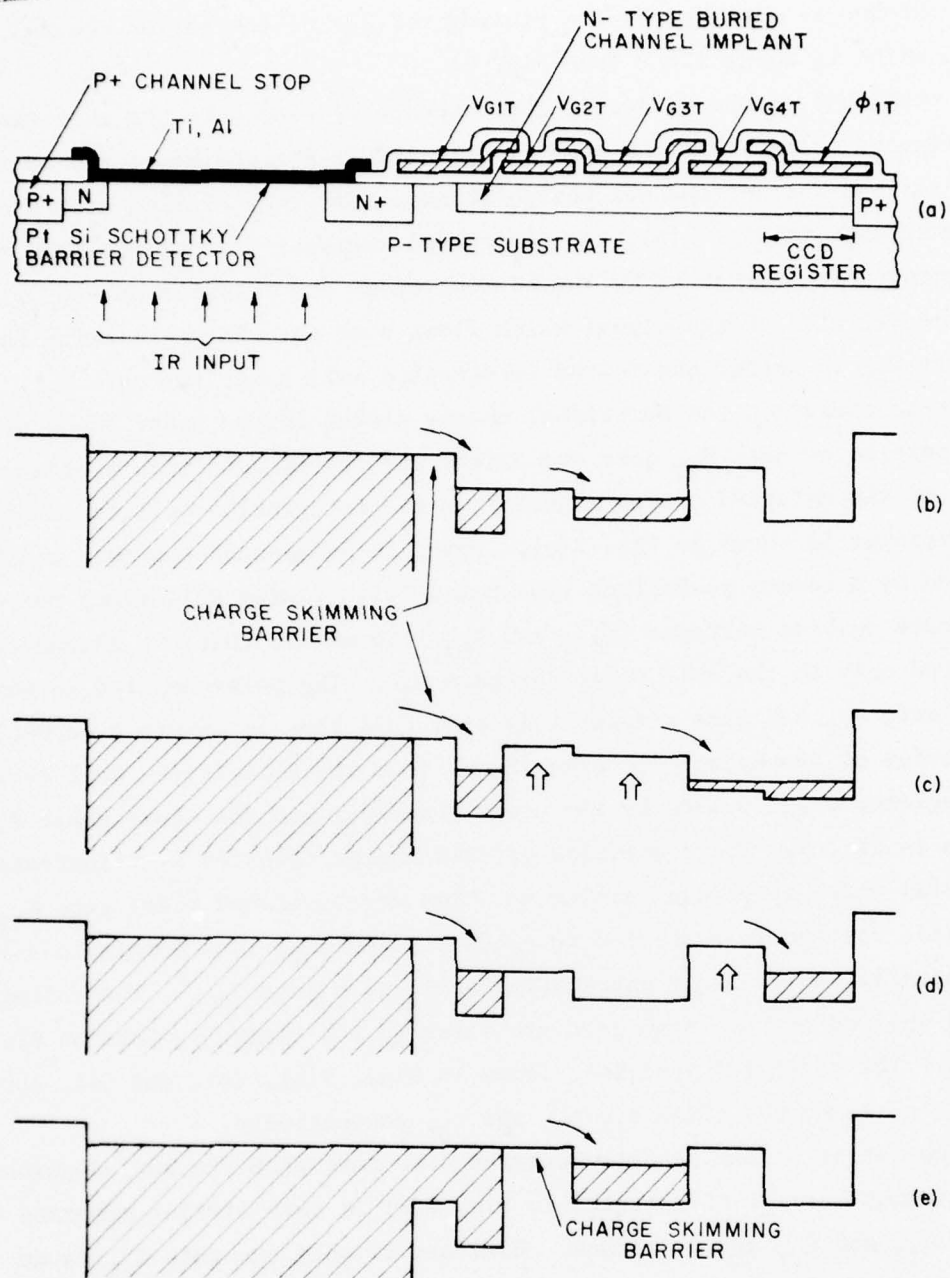
The output registers as well as the charge integration stages were made in the form of buried-channel CCDs. The substrate used was p-type with (100) orientation and resistivity of 20 to 40 ohm-cm. Both sides of the substrate were optically polished. The buried-channel implant was phosphorus with a  $1.3 \times 10^{12} \text{ cm}^{-2}$  dose. The phosphorus implant dose used for the formation of the n-type guard rings surrounding the Schottky diodes was  $1.0 \times 10^{12} \text{ cm}^{-2}$ .

The Schottky-barrier detectors were formed by opening  $8 \times 0.5$  mil Schottky contact holes prior to the metal deposition. The platinum silicide was formed by magnetron sputtering of platinum on the wafers, and then sintering them at temperatures of 650°C or 450°C for 10 or 30 minutes, respectively. The devices were then completed by deposition and definition of titanium aluminum metallization.

#### D. CONTINUOUS CHARGE-SKIMMING MODE

To minimize the noise associated with resetting of the Schottky diodes and to allow for operation with minimum of leakage current (dark current) we designed this array for operation with a "continuous charge-skimming" mode. In this detection mode the Schottky-barrier diode is maintained at a fixed dc bias by a barrier formed under the gate  $G_{1T}$  (shown in Figs. 9(b), (c) and (d) or the gate  $G_{2T}$  (as shown in Fig. 9(e)). The advantage of using a surface-channel region for the charge-skimming barrier controlled by the gate  $G_{1T}$  is that the potential of the Schottky diode can be maintained at any positive voltage arbitrarily close to the substrate potential. Furthermore, the barrier can be set to cut off the conduction channel between the Schottky diodes and the charge-coupling structure, even at room temperature.

The use of the buried-channel as the charge-skimming barrier controlled by gate  $G_{2T}$  (see Fig. 9(e)) may offer a method of operation with somewhat lower noise associated with transferring the charge signal out of the Schottky-barrier detector. But in this mode the minimum positive potential of the



**Figure 9.** Construction and operation of the Schottky-barrier detectors operating in the continuous-charge-skimming mode.

Schottky diodes is dictated by the pinning voltage of the buried channel under gate  $G_{2T}$  which is about 1.6 V (see Fig. 9).

We shall now review in detail the sequence of events in the operation of the continuous charge-skimming mode illustrated in Figs. 9(b), (c), and (d) for the case with a surface-channel charge-skimming barrier. During most of the time illustrated in Fig. 9(b), the CCD output register is isolated from the charge integration structure by the barrier under the transfer gate  $G_{4T}$ . This allows the detected charge signal which flows over the charge-skimming barrier under gate  $G_{1T}$  to accumulate in the integration well under the gate  $G_{3T}$ . In steady-state operation the additional charge packet formed under the buried-channel portion of gate  $G_{1T}$  does not affect the charge detection process. The transfer of the detected charge signal from the integration well to the CCD output register is shown in Fig. 9(c). Here, it is assumed that  $G_{2T}$  and  $G_{3T}$  are pulsed by a common push-clock type pulse (with finite fall time) but with two separate dc bias voltages ( $V_{G2T}$  and  $V_{G3T}$ ) to assure that the charge can be accumulated only in the well under the gate  $G_{3T}$ . The pulse applied to the transfer gate  $G_{4T}$  has also a relatively slow fall time to assure a push-clock type transfer of the detected charge signal from the integration well to the output register stage pulsed by the clock phase  $\phi_{1T}$  and the clock phase  $\phi_{1S}$  not shown in Fig. 9. The completion of this charge transfer is illustrated in Fig. 9(a) where after the barrier has been reestablished under gate  $G_{4T}$ , the positive voltage is reapplied to gates  $G_{2T}$  and  $G_{3T}$ , thus forming a new and essentially empty charge integration well under gate  $G_{3T}$ .<sup>\*</sup> The voltage waveforms applied to the above gate are shown in the timing in Section II.B (Fig. 13). The potential profiles, shown in Figs. 9(b), (c), and (d), correspond in Fig. 13 to the times  $t_1$ ,  $t_2$ , and  $t_3$ , respectively.

The operation of the Schottky-barrier detectors with the buried-channel, charge-skimming barrier illustrated in Fig. 9(e) is very similar provided that the gates  $G_{1T}$  and  $G_{2T}$  are dc biased. However, if only the gate  $G_{1T}$  is dc biased while gate  $G_{2T}$  is pulsed as in the case illustrated by potential profiles in Figs. 9(b), (c) and (d), then the charge-skimming mode will be

<sup>\*</sup>Actually in this case any excess charge that has been accumulated in the well under the buried-channel position of the gate  $G_{1T}$  will be transferred into the charge integration well.

briefly interrupted during the charge transfer process from the charge integration well to the CCD output register. Reapplication of the positive potential to the barrier gate  $G_{2T}$  will, however, reset the Schottky diode back to its charge-skimming potential.

The interesting property of the continuous charge-skimming mode is that the Schottky diodes are maintained at a constant potential which can be adjusted to any desired value by controlling the dc voltage  $V_{GIT}$ . By maintaining the reverse-bias voltage of the Schottky diodes at a low value, the leakage current and the leakage current spikes (which tend to increase exponentially with voltage) can be maintained at minimum levels. However, if desired, the Schottky diode reverse-bias voltage can be increased to a value at which the leakage current spikes become appreciable. Operation with the larger reverse-bias voltage tends to lower the Schottky diodes' photodetection barrier, thus increasing the sensitivity of these devices as thermal sensors.

#### E. DEVICE PACKAGING

The 256-element Schottky-barrier IR-CCDs have been packaged in 30-pin gold-plated flat metal packages, Isotronics IP-1065. The bonded chip is shown in Fig. 10 with labeled electrical pin-out. The photograph in Fig. 11 shows the back-side view of the packaged device. The 420 x 24 mil slot machined in the package is used to illuminate the device through the substrate. As mentioned previously, the back surfaces of the chips are optically polished to avoid light scattering. The metal package used for these devices was found to be a very effective thermal shield for these IR-CCDs.

With the exception of the substrate connection (SUB) to pin No. 1, all other electrical connections to the chip have been illustrated in Fig. 2. Pin No. 1 is connected by one bonding wire to the metal base of the package, and by another bonding wire to the substrate (SUB) pad on the chip. The substrate pad is connected on the chip to the  $p^+$ -diffusion channel stop which extends over all regions of the chip with the exception of the channel regions and the Schottky diode regions (see Figs. 4 and 5).

The total chip visible in Fig. 10 has a size of 444 x 116 mil. The bonded 256-element Schottky-barrier IR-CCD sensor occupies a chip of only 444 x 68 mil. The remaining chip area corresponding to 444 x 48 mil contains

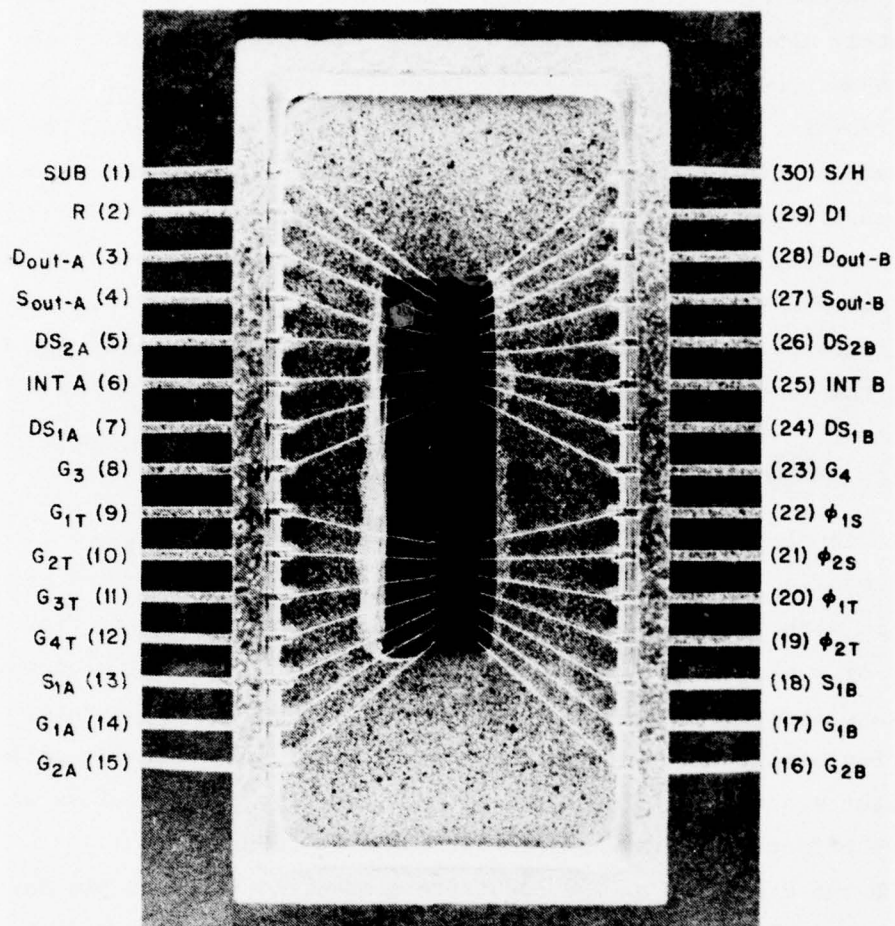


Figure 10. 256-element Schottky-barrier IR-CCD bonded in a 30-pin package.

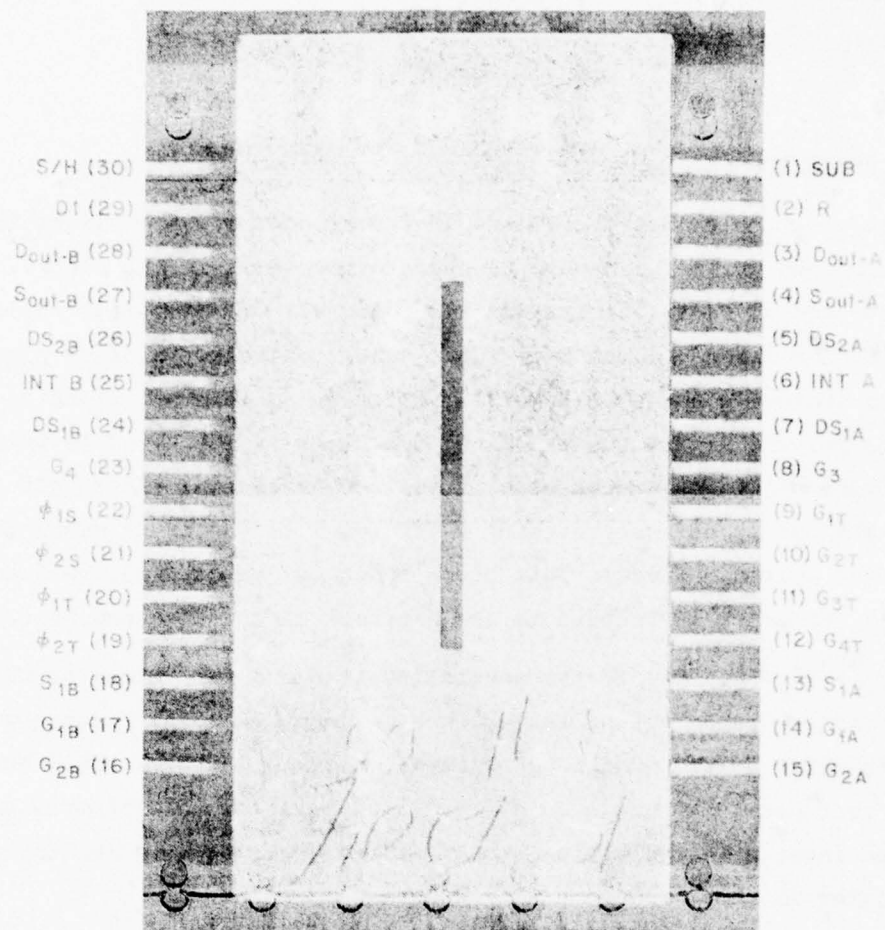


Figure 11. The back-side view of the packaged device of Fig. 10.

an assortment of test devices which were designed for future device development and have not been studied under this contract.

### SECTION III

#### WAVEFORM GENERATOR

##### A. GENERAL OPERATION

The test electronics for the TC1204 IR-CCD scanner provide all of the clock waveforms and dc biases needed to operate the device. The clock waveform amplitude and dc bias, integration time, and all dc potentials applied to the chip may be varied by means of front panel controls. A front panel layout of the tester is shown in Fig. 12. There is an internal clock oscillator in the tester which provides a nominal CCD clock frequency of 10 kHz. However, an external clock may be used if desired by placing the toggle switch to the "EXT CLK" position and providing a TTL level to the front panel BNC adjacent to the switch. (Note: This clock input has an internal 50- $\Omega$  load). The CCD clock frequency is related to the external clock frequency as follows:

$$f_{\text{CCD CLOCK}} = \frac{f_{\text{EXT. CLK}}}{8}$$

Due to the controlled rise and fall times of the CCD clock waveforms generated by the tester, the maximum CCD clock frequency is about 250 kHz which corresponds to an external clock input of 2 MHz. The "SYNC OUT" front panel BNC produces a 4 V, 20- $\mu$ s pulse capable of driving 50  $\Omega$  following the integration (blanking) interval and just prior to reading out the CCD register as shown in the timing diagram, Fig. 13.

The front panel digital voltmeter may be used to monitor any one of 20 adjustable voltages supplied by the tester. Voltmeter selection is made by the combination of the 10-position rotary switch labeled "VOLTMETER" and the adjacent toggle switch labeled "UPR" and "LWR". LED lights located above the voltage controls identify which column the voltmeter is monitoring, and either the upper or lower control in that column is measured depending on the position of the toggle switch. The integration time may be varied from about 1 ms to 1 s in four overlapping ranges by the 4-position rotary switch and the potentiometer located in the upper right corner of the front panel.

Table 1 lists the function of each of the 20 adjustable voltages on the front panel. The adjustment range for each control is listed together with a nominal value for operating the TC1204 at 77 K. These nominal values are intended only as a guide for initially setting up the device since each device

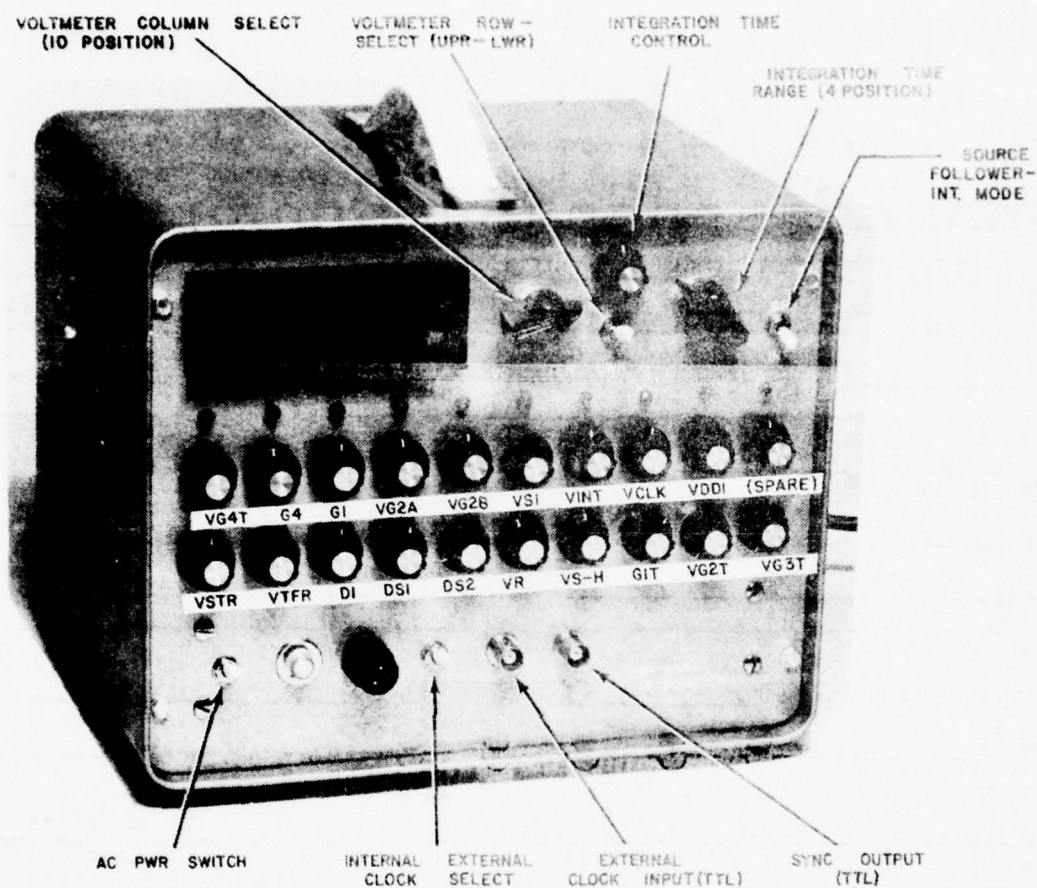


Figure 12. Front panel layout of the waveform generator.

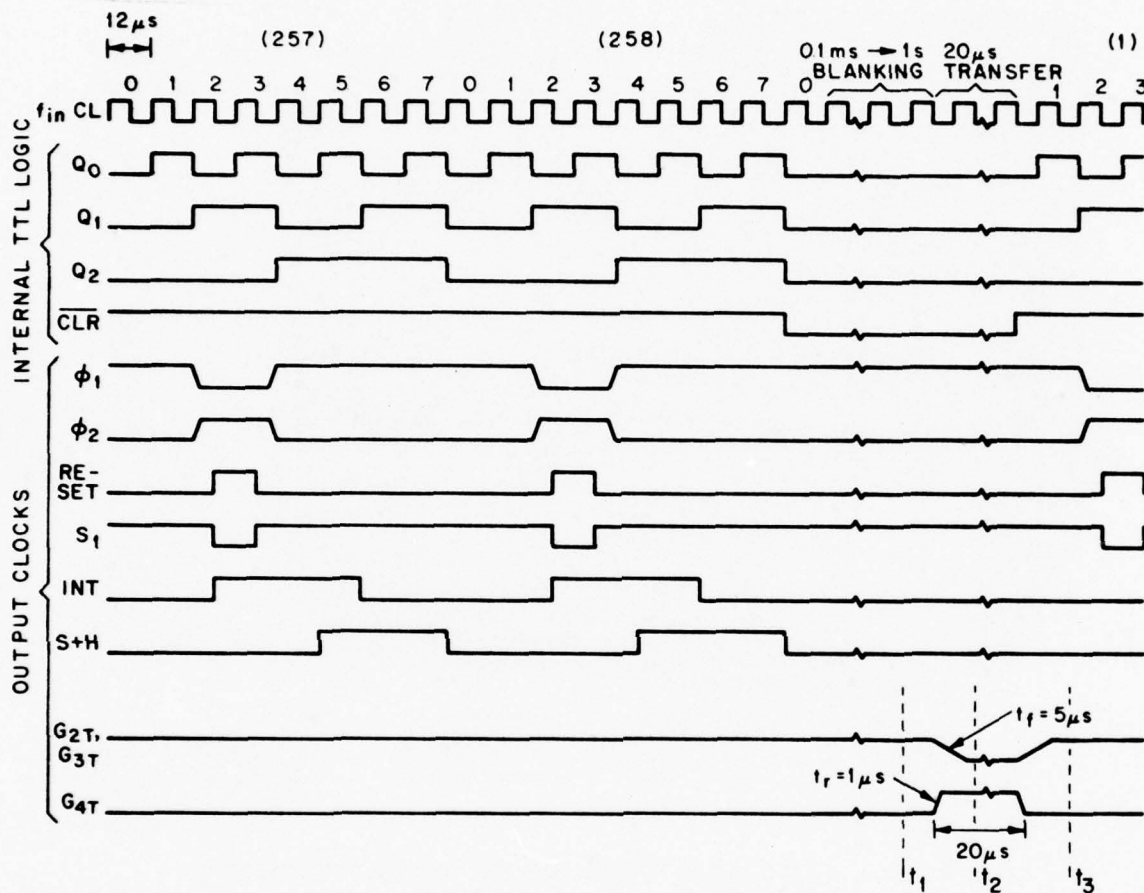


Figure 13. Waveform generator timing diagram.

TABLE 1. BIAS ADJUSTMENTS

CONTROL		FUNCTION	RANGE (VOLTS)	NOMINAL VALUE (77 K)
R1.	VSTR	Storage-Gate Bias ( $\phi_{1S}$ , $\phi_{2S}$ )	-10 to +10	+1.4
R2.	VTFR	Transfer-Gate Bias ( $\phi_{1T}$ , $\phi_{2T}$ )	-10 to +10	-10
R3.	D1	Output-Stage Drains ( $D_1$ , $D_{OUT-A}$ , $D_{OUT-B}$ )	0 to +20	+15
R4.	DS1	Drain-Source #1 ( $DS_{1A}$ , $DS_{1B}$ )	0 to +20	+15
R5.	DS2	Drain-Source #2 ( $DS_{2A}$ , $DS_{2B}$ )	0 to +20	0
R6.	VR	Reset-Gate Bias (R)	-10 to +10	-6
R7.	VSH	Sample + Hold Gate Bias (S/H)	0 to +20	+4.4 (20)
R8.	GI <sub>T</sub>	SCCD-Barrier Gate Bias ( $G_{1T}$ )	-10 to +10	+2 (MIN)
R9.	VG <sub>2T</sub>	BCCD-Barrier-Gate Bias ( $G_{2T}$ )	-10 to +10	-3
R10.	VG <sub>3T</sub>	Charge-Integration-Gate Bias ( $G_{3T}$ )	-10 to +10	-6
R11.	VG <sub>4T</sub>	Parallel-Transfer-Gate Bias ( $G_{4T}$ )	-10 to +10	-5
R12.	G <sub>4</sub>	DC-Output-Gate Bias ( $G_4$ )	-10 to +10	0
R13.	G <sub>1</sub>	Input-Gate Bias ( $G_{1A}$ , $G_{2A}$ )	-10 to +10	-5.5
R14.	VG <sub>2A</sub>	Signal-Input Bias-Register A ( $G_{2A}$ )	-10 to +10	+0.5
R15.	VG <sub>2B</sub>	Signal-Input Bias-Register B ( $G_{2B}$ )	-10 to +10	+0.5
R16.	VS <sub>1</sub>	Charge-Preset Source Bias ( $S_{1A}$ , $S_{1B}$ )	0 to +20	+19
R17.	VINT	Load-Device Gate Bias (INT-A, INT-B)	0 to +20	+5
R18.	VCLK	Main-Clock Amplitude ( $\phi_{1S}$ , $\phi_{1T}$ , $\phi_{2S}$ , $\phi_{2T}$ , $S_{1A}$ , $S_{1B}$ , R, $G_{2T}$ , $G_{4T}$ )	0 to +20	+10
R19.	VDDL	Aux.-Clock Amplitude (INT, S/H)	0 to +20	+3 + +10
R20.	(SPARE)			

may require slightly different bias values due to differences in thresholds, etc.

#### B. CLOCK WAVEFORM TIMING

The TC1204 waveform generator supplies the clock waveforms shown in the timing diagram, Fig. 13. The master clock input  $f_{IN}$  may be either the internally supplied clock oscillator or an external TTL clock applied to the front panel BNC connector. The TC1204 timing cycle is comprised of these periods: (1) the serial-register readout period, (2) the blanking or integration time period, and (3) the parallel transfer period. During the serial register readout period the waveform generator produces 258 cycles at the CCD clock rate  $\phi_1, \phi_2$  (this corresponds to  $8 \times 258 = 2064$  cycles of the master clock). Although there are only 256 Schottky-barrier detectors, 258 clock cycles are produced during readout to account for the extra 2-bit delay needed for synchronization when the serial output of the Register A is fed back directly to the serial input of the Register B. This is useful when the TC1204 is configured for a motion detector system using a difference output A-B. Following the serial-register readout period is a blanking (or integration) time period which is variable from about 0.1 ms to 1 s, using the front panel integration time switch and variable potentiometer controls. During this blanking time all of the output clocks are inhibited and signal charge from the Schottky-diode detector is being collected under the charge integration gate  $G_{3T}$ . Since, however, signal charge from the Schottky diodes is also collected under  $G_{3T}$  during the output-register readout period, the effective integration time is actually the sum of the serial-register readout period and the blanking period. Following the blanking period, the 20- $\mu$ s pulses applied to  $G_{2T}$ ,  $G_{3T}$ , and  $G_{4T}$  transfer the integrated signal charge under  $G_{3T}$  in parallel to the Output Register A.

The CCD clocks  $\phi_1$  and  $\phi_2$  produced by the TC1204 waveform generator are symmetrical, overlapping, 2-phase clocks. These clock waveforms are applied to the CCD phase electrodes  $\phi_{1S}$ ,  $\phi_{1T}$ ,  $\phi_{2S}$ , and  $\phi_{2T}$  via dc restoring circuits so that the dc level applied to the storage gates  $\phi_{1S}$  and  $\phi_{2S}$  is controlled by  $V_{STR}$  and the dc level applied to the transfer gates  $\phi_{1T}$  and  $\phi_{2T}$  is controlled

by  $V_{TFR}$ . The remaining output clocks  $R$ ,  $S_1$ ,  $INT$ ,  $S/H$ ,  $G_{2T}$ ,  $G_{3T}$ , and  $G_{4T}$  are also applied via dc restoring circuits, each with an independent bias control.

The reset pulse  $R$  resets the output floating diffusions to the potential on  $D_1$  when  $\phi_1$  is off. At the same time, the negative going pulse on  $S_1$  performs the charge preset function at the serial register inputs when electrical input is desired. At the positive going edge of  $\phi_1$  (following the reset pulse) signal charge is transferred to the floating diffusion. The information present at the floating diffusion is then sampled by the  $S/H$  pulse applied to the gates of sampling transistors  $Q_7$  and  $Q_8$  shown in Fig. 8.

### C. TC1204 WAVEFORM GENERATOR CIRCUIT DESCRIPTION

Detailed schematic diagrams for the TC1204 waveform generator are shown in Figs. 14 to 16. Referring first to printed-circuit board #1 (PCB #1), Fig. 14, all of the internal timing waveforms are derived from the master clock using standard TTL logic. The TTL logic levels are then translated to variable amplitude clock waveforms using MH0026 clock driver ICs. The internal clock oscillator is a voltage-controlled Schottky TTL oscillator SN74LS324. It produces a square-wave output frequency at nominally 80 kHz, which may be varied over about a 2:1 range by adjustment of the trimmer pot  $R1$  mounted on PCB#1. The value of capacitor  $C1$  determines the midpoint of this range. An external TTL clock may be used by switching  $S_1$  to the EXT position. The duty cycle of the external clock is not critical since it is divided down internally. The master clock  $f_{IN}$  is applied to a synchronous 4-stage binary counter  $U1$  (74161) which generates the timing waveforms  $Q_0$ ,  $Q_1$  and  $Q_2$  shown in the timing diagram. (Note: only 3 stages of this counter are utilized to divide by 8).  $\overline{Q_2}$ , which is at the CCD clock rate, is used to clock the synchronous 4-stage binary counters  $U2$  and  $U3$ .  $U2$  and  $U3$  are used to divide  $Q_2$  by 256. The required division by 258 is obtained by sensing the  $U3$  last stage negative transition (which occurs after 256 cycles) with a D-type flip-flop  $U7(1)$  and applying the output of  $U7$  (pin 5) together with the  $\div 2$  output of  $U2$  (pin 13) to a NAND gate  $U4$ . Thus, following 258 cycles of  $Q_2$ ,  $U4$  (pin 3) switches low which triggers the blanking time one-shot  $U10(1)$  and also initiates a  $\overline{CLR}$  pulse which resets all of the counters. The  $\overline{CLR}$  pulse holds the counters  $U1$ ,  $U2$ , and  $U3$  reset until the blanking time and transfer time one-shots (which are part of the dual monostable  $U10$  74123)

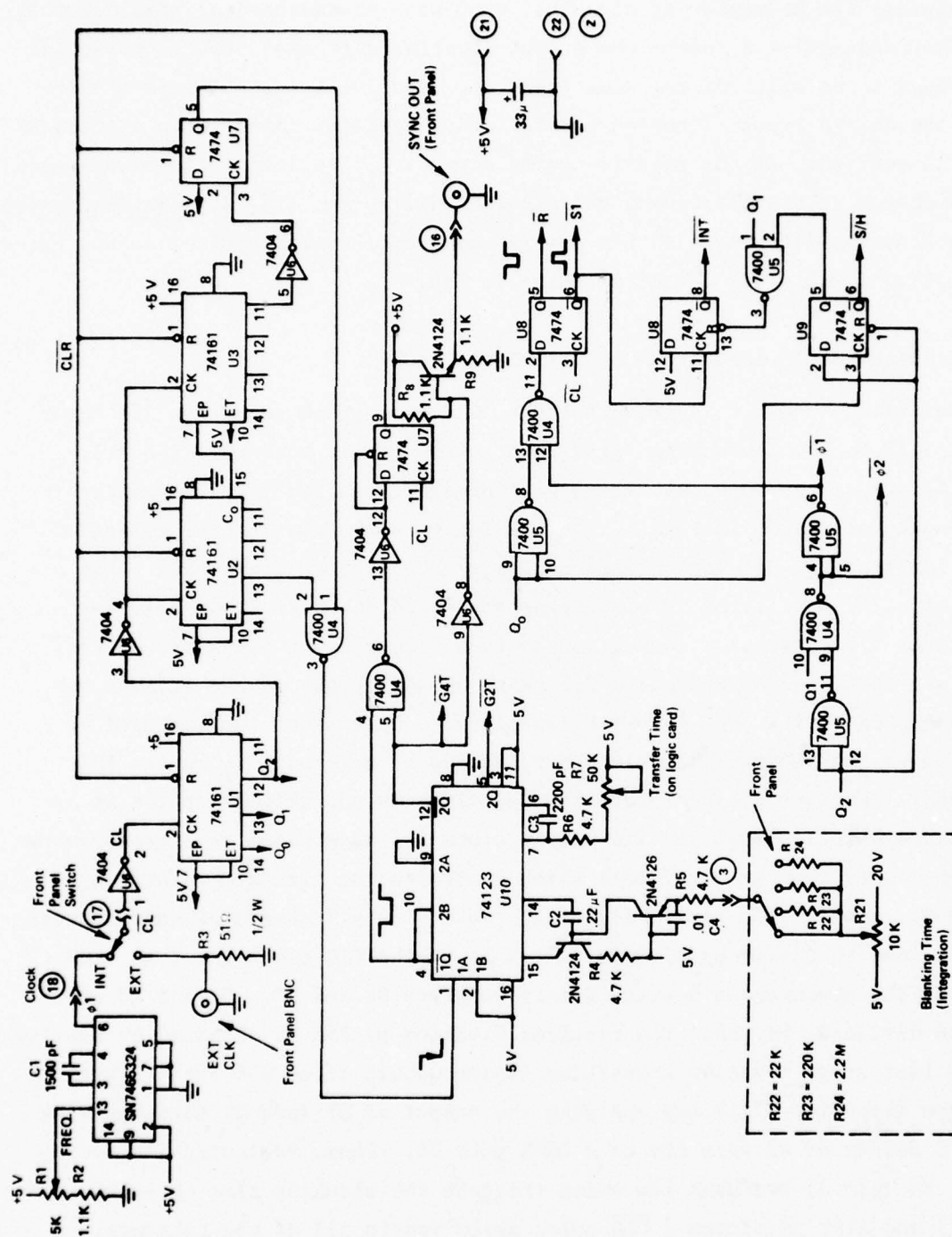


Figure 14. (a) Printed-Circuit Board No. 1.

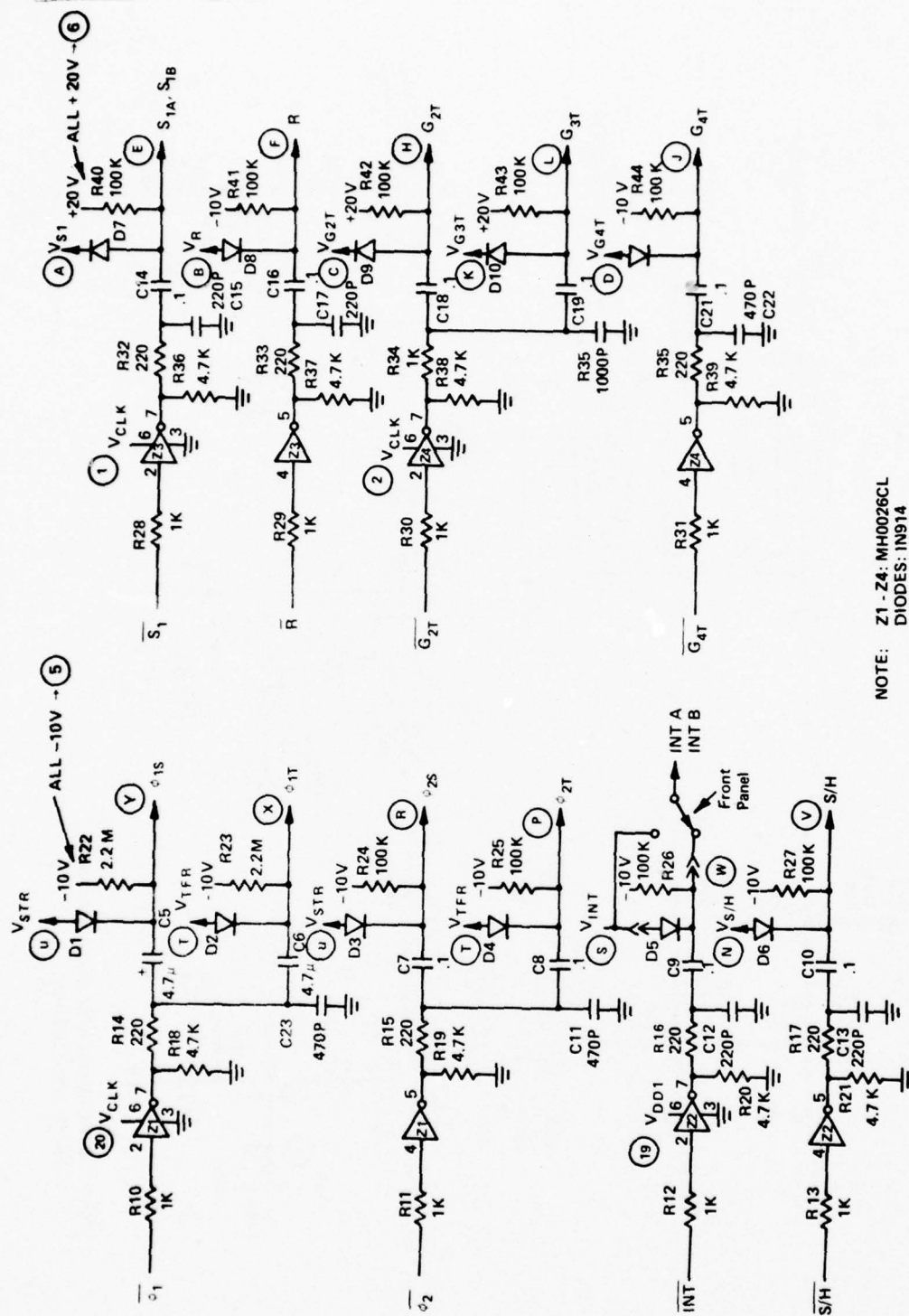
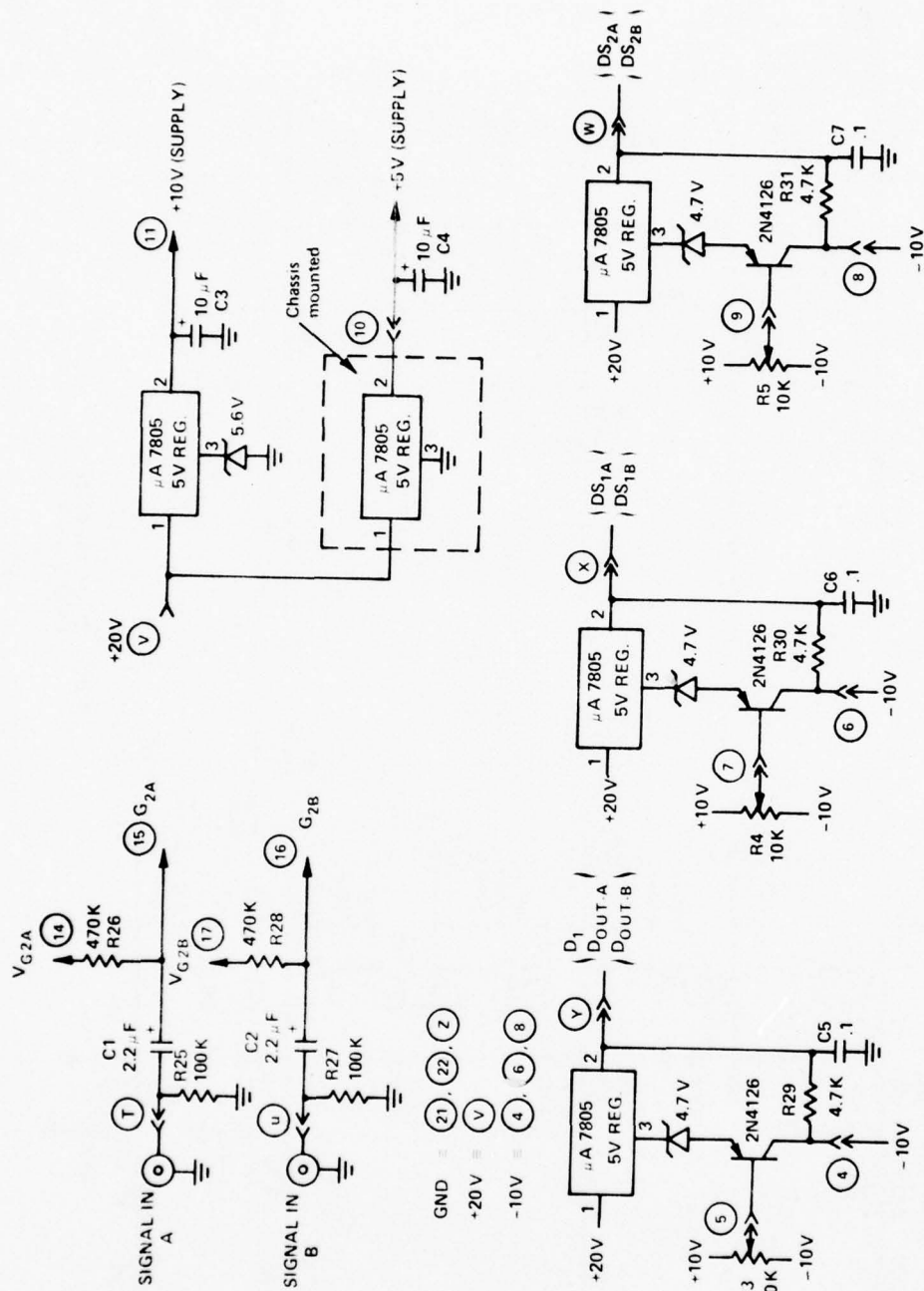
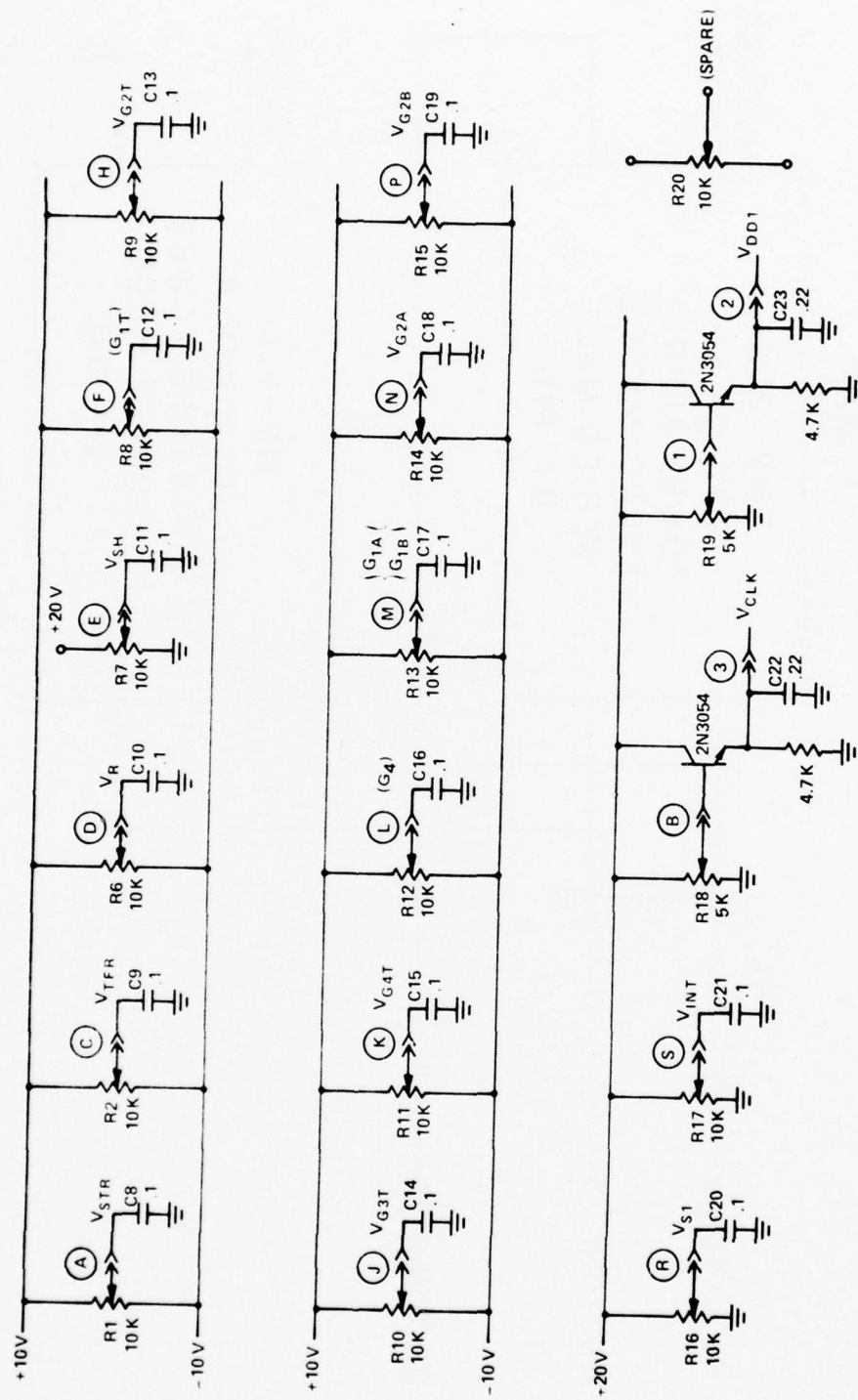


Figure 14. (b) Printed-Circuit Board No. 1 (Continued).



NOTE: R3, R4, R5 MOUNTED ON FRONT PANEL  
R4, R5 10KΩ, 10-TURN

Figure 15. (a) Printed-Circuit Board No. 2.



NOTE: R1, R2, R6 - R19 MOUNTED ON FRONT PANEL  
R8, R9: 10K $\Omega$ , 10-TURN

Figure 15. (b) Printed-Circuit Board No. 2 (Continued).

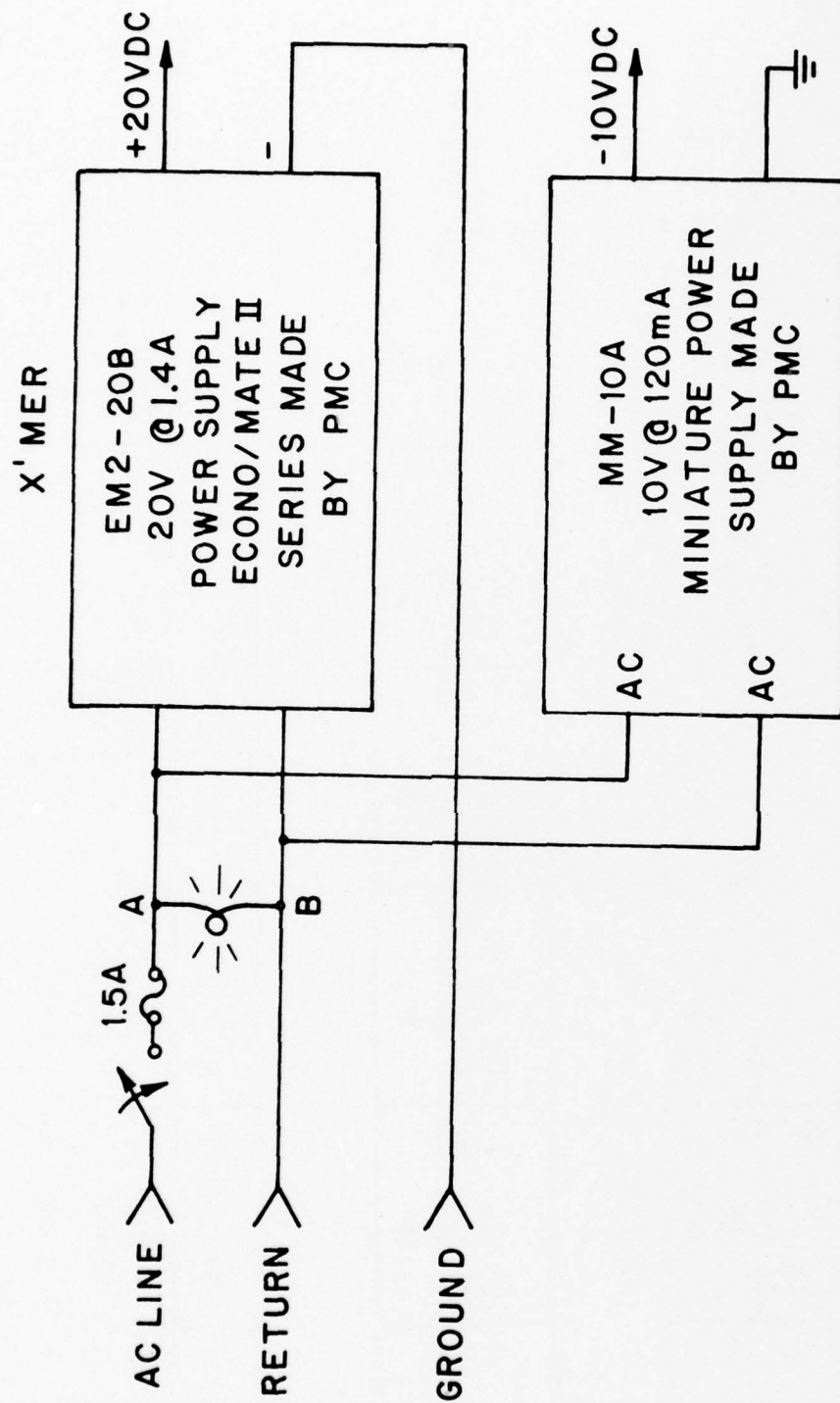


Figure 16. Main power supply wiring diagram.

time out. A synchronous start-up for the next readout period is assured by synchronizing the end of the  $\overline{\text{CLR}}$  pulse using the flip-flop U7(pin 12) which is clocked by  $\overline{\text{CL}}$ . The  $\phi_1$  and  $\phi_2$  (i.e.,  $\overline{\phi_1}$ ) clocks are derived logically from  $Q_1$  and  $Q_2$  according to the Boolean function  $\overline{\phi_1} = Q_1 \cdot \overline{Q_2}$ . The reset and  $S_1$  pulses are derived by delaying the function  $\overline{Q_0} \cdot \overline{\phi_1}$  by 1/2 clock cycle in flip-flop U8(pin 2). The other waveforms are derived using similar techniques.

The TTL level signals  $\overline{\phi_1}$ ,  $\overline{\phi_2}$ ,  $\overline{S_1}$ ,  $\overline{R}$ ,  $\overline{G_{2T}}$ , and  $\overline{G_{4T}}$  are translated to the level of VCLK by MH0026 clock driver IC's Z1, Z3, and Z4. The TTL level signals  $\overline{\text{INT}}$  and  $\overline{\text{S/H}}$  are translated to the level of  $V_{\text{DD1}}$  by a separate MH0026 driver Z2. The inputs to the MH0026 drivers are isolated with 1-k $\Omega$  resistors to prevent excessive loading to the TTL voltage high levels. The MH0026 output rise and fall times are slowed by RC integrator circuits (e.g., R15, C11) to minimize capacitively coupled transients between the various clock lines. The outputs are then dc-restored with diode clamping circuits (e.g., C5, D1, R22). Output clocks,  $\phi_{1S}$ ,  $\phi_{1T}$ ,  $\phi_{2S}$ ,  $\phi_{2T}$ , INT, S/H, R, and  $G_{4T}$  are clamped to the negative level of the waveforms. Output clocks  $S_1$ ,  $G_{2T}$ , and  $G_{3T}$  are clamped to the positive level of the waveforms.

Printed-circuit board #2 (PCB#2) contains the variable dc bias power supplies needed for the waveform generator. These variable supplies include current limiting so that accidental shorting of pins at the TC1204 device socket will not damage the waveform generator under normal circumstances.

The main power supplies for the waveform generator are shown in Fig. 16 and include a 20 V at 1.4 A supply and a -10 V at 120-mA bias supply. Both power supplies are manufactured by POWER/MATE Corporation.

The wiring connections between the cable connector for the TC1204 package and the two printed circuit boards are listed in Table 2. Note that pin No. 4,  $S_{\text{OUT-A}}$ , and pin No. 27,  $S_{\text{OUT-B}}$ , require external 10-k $\Omega$  terminations to ground.

TABLE 2. CABLE CONNECTOR WIRE LIST

CABLE CONNECTOR PIN #	BOARD CONNECTION
1. SUBSTRATE	GROUND
2. R	XA1-F
3. D <sub>OUT-A</sub>	XA2-Y
4. S <sub>OUT-A</sub>	□
5. DS <sub>2A</sub>	XA2-W
6. INT-A	INTSW
7. D <sub>S1A</sub>	XA2-X
8. G <sub>3</sub>	XA1-X
9. G <sub>1T</sub>	XA2-F
10. G <sub>2T</sub>	XZ1-F
11. G <sub>3T</sub>	XA1-L
12. G <sub>3T</sub>	XA1-J
13. S <sub>1A</sub>	XA1-E
14. G <sub>1A</sub>	XA2-M
15. G <sub>2A</sub>	XA-2-15
16. G <sub>2B</sub>	XA2-16
17. G <sub>1B</sub>	XA2-M (14)
18. S <sub>1B</sub>	XA1-E (13)
19. $\phi_{2T}$	XA1-P
20. $\phi_{1T}$	XA1-X (8)
21. $\phi_{2S}$	XA1-R
22. $\phi_{1S}$	XA1-Y
23. G <sub>4</sub>	XA2-L
24. DS <sub>1B</sub>	XA2-X (7)
25. INT <sub>B</sub>	INTSW (6)
26. DS <sub>2B</sub>	XA2-W (S)
27. S <sub>OUT-B</sub>	□
28. D <sub>OUT-B</sub>	XA2-Y (3)
29. D1	XA2-Y (3)
30. S/H	XA1-V

NOTE: XA1  $\equiv$  PC Board #1XA2  $\equiv$  PC Board #2□  $\equiv$  with 10 k $\Omega$  load to ground and coax RG 174.

## SECTION IV

### DEVICE OPERATION AND EXPERIMENTAL RESULTS

#### A. ELECTRICAL OPERATION

The circuit diagram for operation of the 256-element IR-CCD sensor with the tester described in Section III is shown in Fig. 17. The nominal settings of the voltage controls of the tester have been shown in Table 1. The following sections will review how the operation of the device should be effected by tester control settings, and typical electrical performance will be given.

##### 1. Voltage Level Control of the Schottky-Barrier Diodes

The voltage level of the Schottky-barrier diodes is controlled either by the surface-channel (SCCD) barrier gate  $G_{1T}$  or by the buried-channel (BCCD) barrier gate  $G_{2T}$ .

For operation of the output registers at room temperature, the Schottky-barrier diode must be isolated from the CCD structure by cutting off the channel under the gate  $G_{1T}$ . Typical surface-channel threshold voltages of the tested devices at room temperature were measured to be between 0.86 and 1.12 V. The above values were determined by adjusting the dc bias voltage  $G_{1T}$  to the minimum positive value at which small signal spikes start appearing at the output. This output waveform is shown at room temperature for one device in Fig. 18. The output response to an externally applied input to Register A is also present in this photograph for comparison. The value of the dc voltage applied to the gate  $G_{1T}$  was 1.16 V. The variation of the detected output signal in this test corresponds to the variation of the MOS thresholds in the surface channel sections between the Schottky-barrier diodes and the buried-channel CCD structure. Similar tests made at 77 K showed a typical surface channel threshold under the gate  $G_{1T}$  of about 1.9 V.

##### 2. Leakage Current of Buried-Channel CCD at 300 K

To measure the leakage current (dark current) of the CCD readout structure, the surface-channels connecting to the  $n^+$ -diffusions in contact with the Schottky diodes were cut off by adjusting the dc voltage applied to  $G_{1T}$  to less

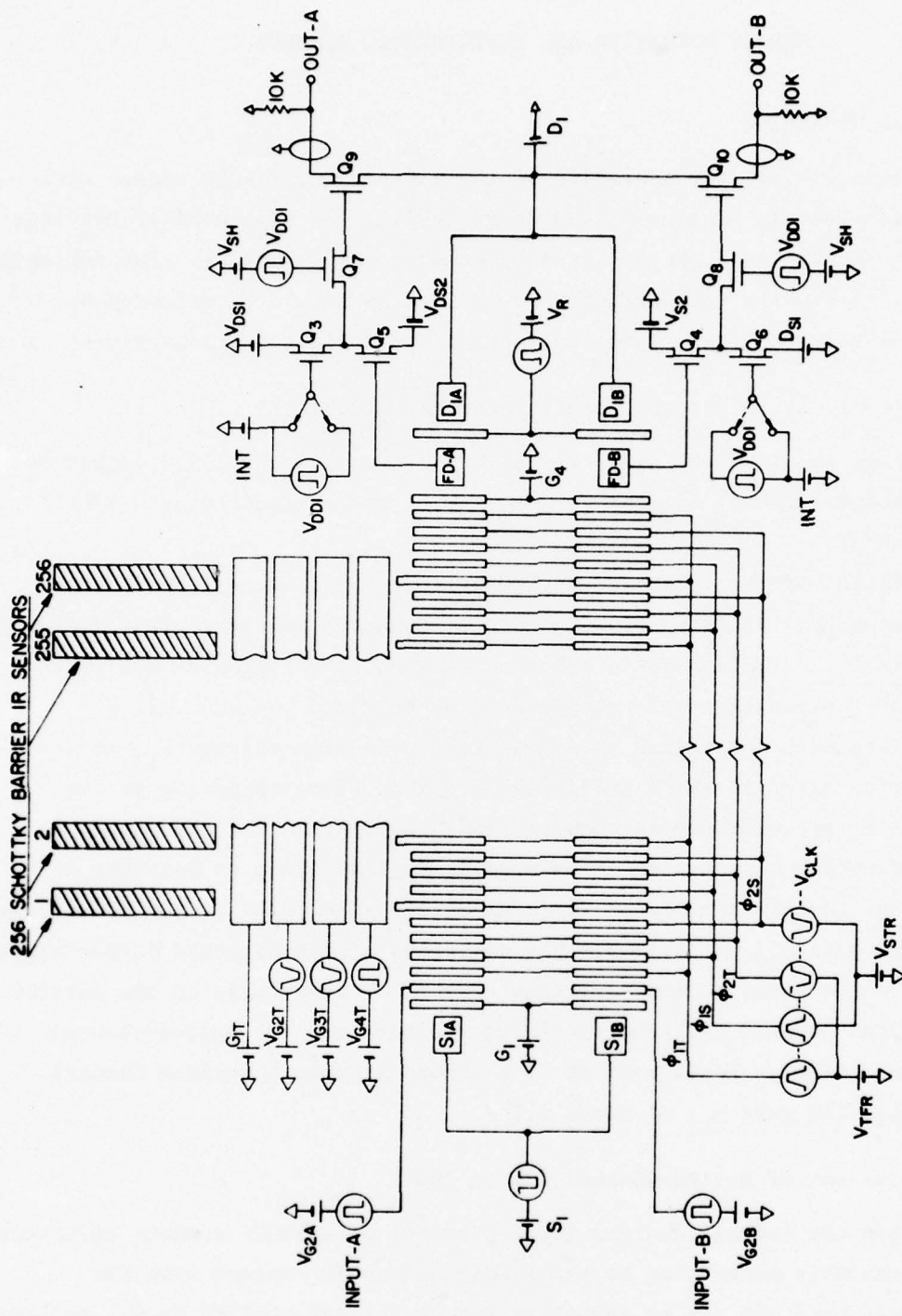


Figure 17. Circuit diagram for operation of the 256-element IR-CCD sensor.

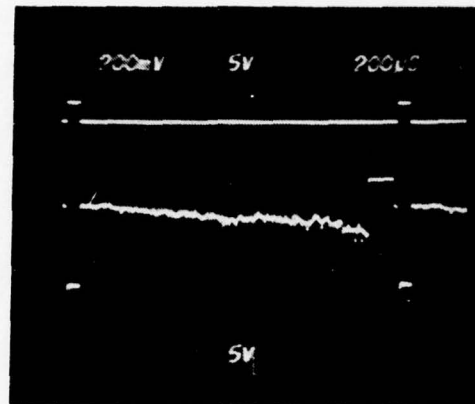


Figure 18. Waveforms of the input and the output at 300 K for dc voltage applied to gate  $G_{1T}$  of 1.16 V. The top trace is the applied input to Register A (5 V/div). The bottom trace is the detected Output A-B (200 mV/div).

than 0.8 V. A typical dark current output waveform obtained for 100 ms integration is shown in Fig. 19. The detected signal in this figure is the difference between the channel A and the channel B. Therefore, this waveform shows the dark current generated in Register A plus the dark current generated in the buried channels under the gates  $G_{2T}$ ,  $G_{3T}$ , and  $G_{3T}$  minus the dark current generated in Register B. Assuming about the same dark current density in all buried-channel regions of the two output registers, the measured dark current corresponds to an area of  $2.32 \text{ mil}^2$  of the buried-channel regions connecting the Schottky diodes with Register A. For an integration time of 100 ms, output amplifier gain of 0.55, and estimated capacitance of the floating diffusion of 0.19 pF, the average dark current of the buried channel operating at minimum voltage of about 1.6 V (see Fig. 19) is  $0.6 \text{ pA/mil}^2$  or  $93 \text{ nA/cm}^2$ .

### 3. Leakage Current of Schottky-Barrier Diodes at 77 K

The leakage (dark) current of the platinum silicide Schottky barrier diodes has been measured at 77 K. For these measurements the devices were immersed in liquid nitrogen and a special care was taken to provide a good thermal shield for the devices.

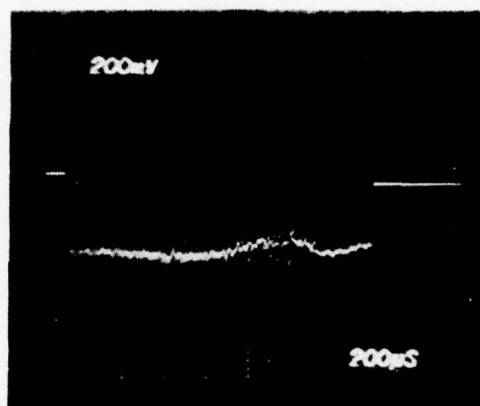
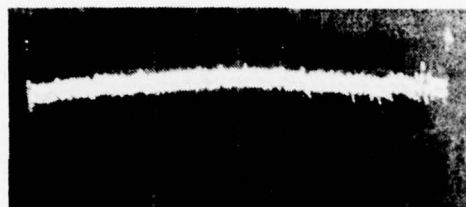
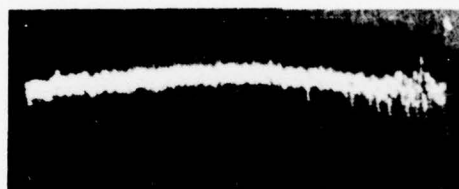


Figure 19. Waveform of dark current of the buried-channel CCD at 300 K. The output is detected as Output A - Output B (200 mV/div).

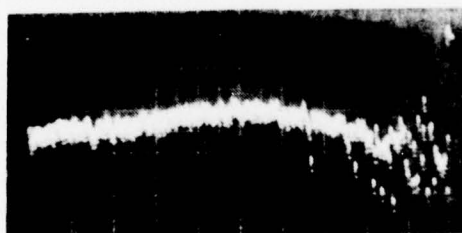
The waveforms of the detected leakage current of the Schottky diodes at different dc voltages applied to the skimming barrier gate  $G_{1T}$  are illustrated in Fig. 20. For these waveforms, the charge integration time was 250 ms. The curve of the Schottky-barrier diode leakage current density as a function of the dc bias applied to the gate  $G_{1T}$  is shown in Fig. 21, assuming that  $C_{FD} = 0.19$  pF. Since the channel threshold voltage under gate  $V_{G1T}$  at 77 K is about 2 V, the actual reverse-bias voltage applied to the Schottky-barrier device is about 2 V less than the value of  $V_{G1T}$ . The data in Fig. 21 show that, at 77 K for a reverse-bias voltage of 1.5 V and less, the leakage current density of the platinum silicide Schottky-barrier diodes is  $8.8 \times 10^{-15}$  A/mil<sup>2</sup> or  $1.4 \times 10^{-9}$  A/cm<sup>2</sup>. In the device for which the data are given in Figs. 20 and 21, the leakage current spikes became noticeable as the voltage  $V_{G1T}$  was increased above 5 V. For  $V_{G1T}$  larger than 8 V the leakage current output became very spiky and rapidly increased with voltage  $V_{G1T}$ . It should be noted, however, that other devices were measured where no appreciable increase of the leakage current was observed for Schottky-barrier diodes operating at 77 K, 100 ms integration time, and reverse-bias voltages in excess of 10 V.



(a)



(b)



(c)

Figure 20. Waveform of the leakage current of the PtSi Schottky-barrier devices at 77 K as a function of the skimming-barrier gate dc bias voltage,  $V_{G1T} = 3.5$  V in (a);  $V_{G1T} = 4$  V in (b); and  $V_{G1T} = 5.0$  V in (c). The integration time is 250 ms, and the vertical scale is 20 mV/div.

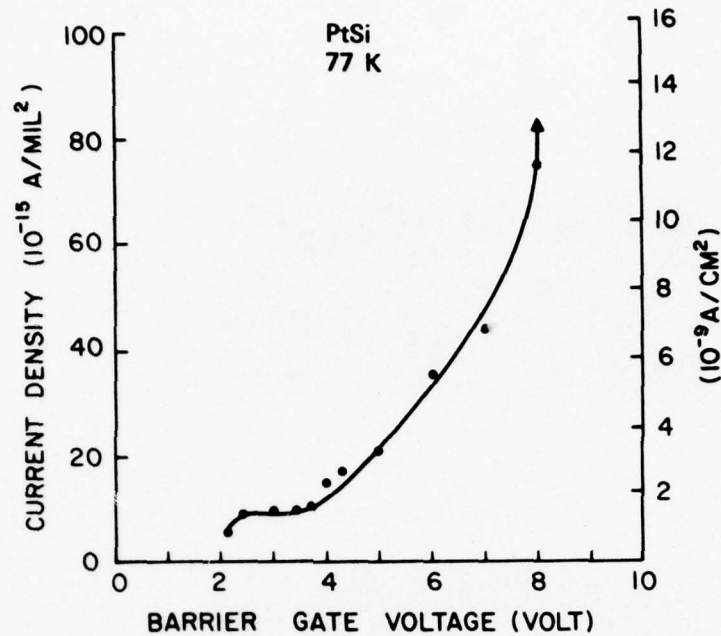


Figure 21. Measured leakage current of PtSi Schottky-barrier diodes at 77 K.

#### 4. Operation of the Output Registers

(a) *Inputs* - The dual-output registers operated with the waveform generator described in Section III have a charge-preset input, also known as a fill-and-spill input. The basic operation of this type of input is illustrated in Fig. 7. The input-charge metering well in this case is formed under the input gate  $G_2$  with the channel potential under the input gate  $G_1$  forming the overflow barrier. To make sure that this input operates properly, the dc bias voltage  $G_1$  common to both channels should be adjusted at some value more positive than the transfer gate bias voltage  $V_{TFR}$  by about 2.0 V. This will assure that the barrier voltage under gate  $G_1$  will be lower (more positive) than under the first transfer gate controlled by  $\phi_{1T}$  (see Fig. 7). The input-source bias voltage  $V_{S1}$  is set first to  $V_{S1} = +20$  V, or a large enough positive value to cut off the input. Then,  $V_{S1}$  is adjusted to a voltage about 1.0 V less positive than the value required to start introducing the signal into the charge metering well. The value of the input charge, then, can be determined by the voltage applied to gates  $G_2$ . The input charge bias levels of the two

channels, i.e., the "fat zeros," are determined by voltages  $V_{G2A}$  and  $V_{G2B}$ . The variable charge inputs are controlled by externally applied signals Input A and Input B. Control of the dc voltage  $G_1$  applied to the gates  $G_{1A}$  and  $G_{1B}$  can also be used to simultaneously adjust the bias levels of the input charge applied to both output channels.

(b) *Operation of the 256-stage registers* - The proper operating voltages for the phase clocks of the output registers can be predicted from the data on the buried-channel potential variations under the two levels of polysilicon gates as a function of the gate voltages [4]. Such data is shown in Fig. 22. The

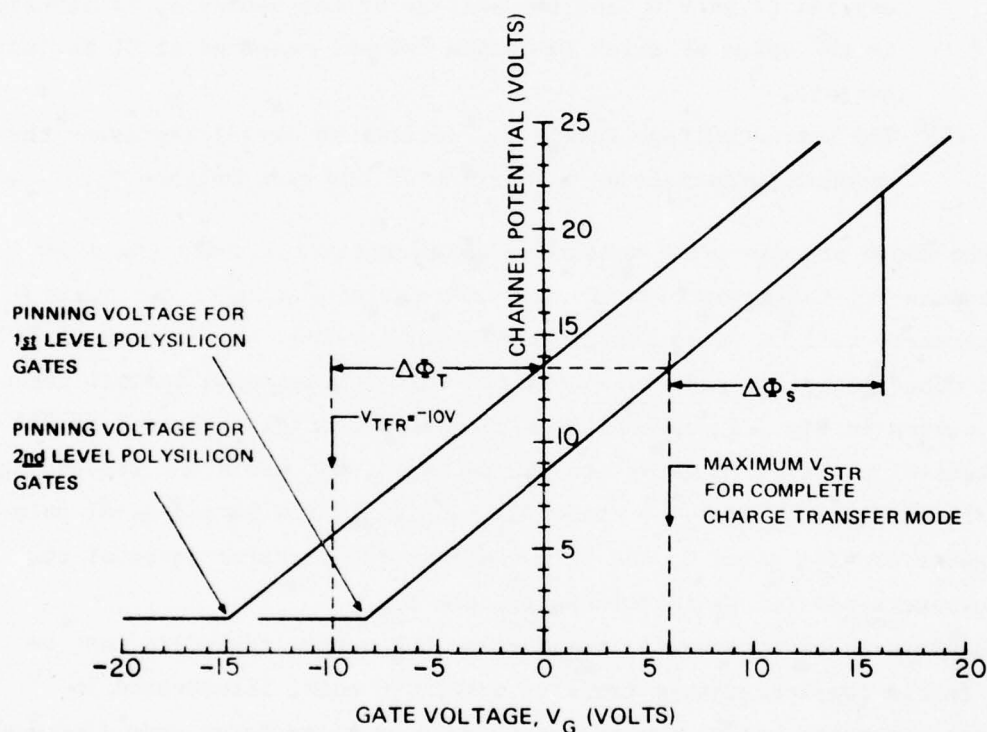


Figure 22. Potential of the buried channels under the first and the second level of polysilicon gates as a function of the gate voltage at 300 K.

4. W. F. Kosonocky and J. E. Carnes, "Two-Phase Charge-Coupled Devices with Overlapping Polysilicon and Aluminum Gates," RCA Review 34, 164, (1973).

curves given for the operation at 300 K were measured by 256-stage registers using the following procedure:

- (1) All the gates of the 256-stage register are turned on by application of large positive voltage (such as +20 V) with the exception of the gate whose channel potential is to be measured. This includes all the clock gates, the gates  $G_3$  and  $G_4$ , and the reset gate R.
- (2) A large positive voltage is also applied to the drain D-1.
- (3) Assuming that the channel potential is measured under the input gate  $G_1$  (this should represent, in general, the channel potential of the second-level polysilicon gates), a given dc voltage  $V_G$  is applied to gate  $G_1$  and the voltage of the source  $S_1$  is adjusted to the value at which the drain current measured at D1 is just cut off.
- (4) The source voltage levels  $V_{S1}$  determined in (3) represent the channel potentials as a function of the gate voltage  $V_G$ .

In the above procedure the measured channel potential under the given gate just cuts off the conduction channel from the source  $S_1$  to the drain  $D_1$ . This measurement will be valid only if the drain and the channel potentials under all other gates are made more positive than the measured channel potential.

The curves in Fig. 22 represent the channel potentials measured at 300 K. The first-level polysilicon gates are the gates  $G_2$ ,  $G_4$ , and R and the storage gates of the register powered by clocks  $\phi_{1S}$  and  $\phi_{2S}$ . The second-level polysilicon gates are the gates  $G_1$  and  $G_3$  as well as the transfer gates of the output registers powered by the clocks  $\phi_{1T}$  and  $\phi_{2T}$ .

To achieve best performance, the 2-phase CCD output registers must be operated in the complete charge transfer mode, C-C mode, illustrated in Fig. 23(a). In other words, the bucket-brigade or bias-charge mode (B-B mode) illustrated in Fig. 23(b) should be avoided [5]. On the basis of the data in Fig. 22, with operation at 300 K, clock-voltage amplitude  $V_{CLK} = 10$  V, and

5. W. F. Kosonocky and J. E. Carnes, "Basic Concepts of Charge-Coupled Devices," RCA Review 36, 566, (1975).

transfer gate bias  $V_{TFR} = -10$  V, operation in the C-C mode requires that the storage gate bias  $V_{STR}$  be less than +6 V. The test of the transition from the C-C mode to the B-B mode at 77 K was measured at  $V_{STR} = +3.82$  V, also for  $V_{CLK} = 10$  V and  $V_{TFR} = -10$  V.

Referring back to Fig. 22, the corners on the left-hand side of the curves represent the buried-channel pinning voltages for the first polysilicon and the

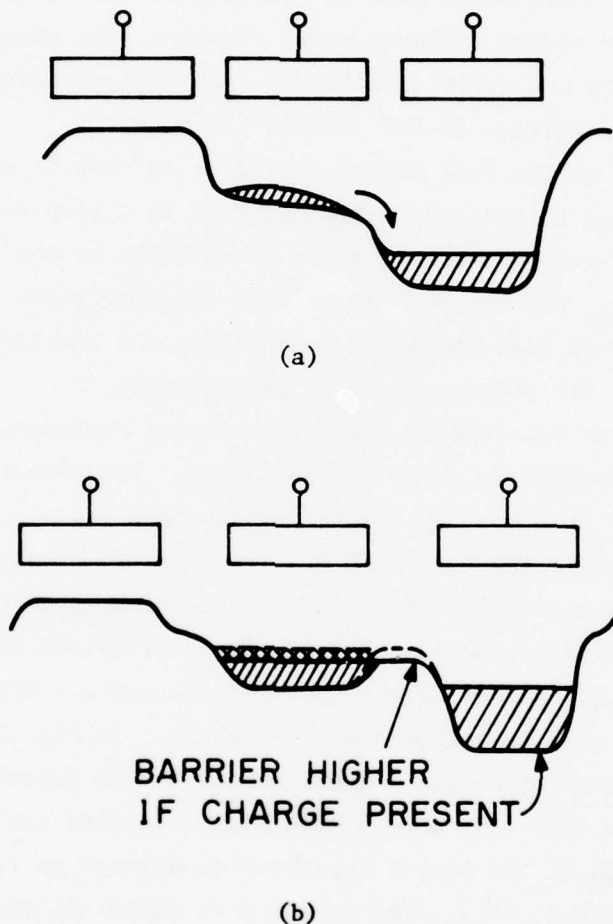


Figure 23. Charge-transfer modes of operation:  
 (a) complete charge-transfer (C-C mode);  
 (b) bucket-brigade or bias-charge (B-B mode).

second polysilicon gates of -15 V and -8.5 V, respectively. The channel potential of 1.6 V at pinning is the lowest possible in the buried-channels of these devices [4].

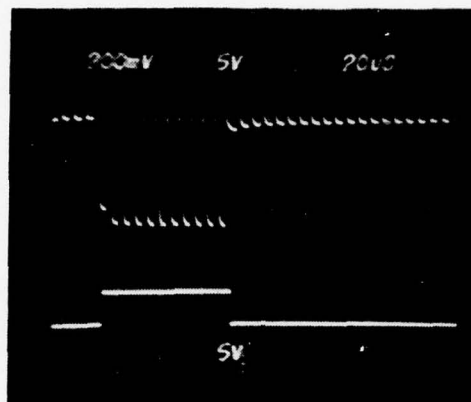
(c) *Output Amplifiers* - As was illustrated in Fig. 17, the first stage of the dual-output amplifier could be operated either in the integration mode (INT) or in the source follower mode (SF). All of the data reported in this report, however, were measured in the source-follower mode. Initial tests showed that for 10 kHz clock the integration mode is capable of about five times higher voltage gain than the source follower mode. However, the waveform generator in the present form is not quite suitable to take full advantage of the operation of the output amplifier in the integration mode.

Another feature of the dual output amplifier is that it can be operated with a direct coupling to the second amplifier or in a sample-and-hold mode. The amplitude of the output sampling pulse is adjusted by the auxiliary clock-amplitude control  $V_{DD1}$  and the dc bias of this sampling pulse by  $V_{SH}$  (see Fig. 17). The separate bias amplitude control for the sampling pulse has been provided to minimize the associated clock feedthrough.

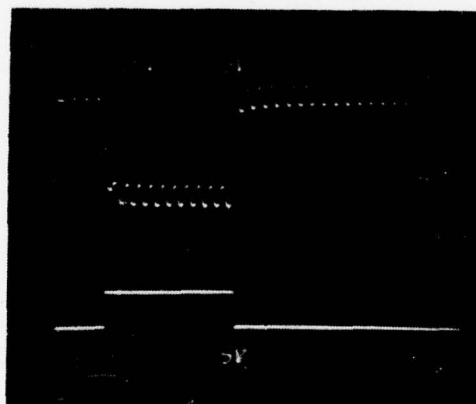
Typical waveforms detected by one of the output amplifiers for the direct coupling mode of operation is shown in Fig. 24(a). The direct coupling mode has been obtained in this case by increasing the bias voltage  $V_{SH}$  to a maximum positive value and adjusting  $V_{DD1}$  to 0 V. The decrease of the clock feedthrough by operating the output amplifiers in the sample-and-hold mode is shown for comparison with the direct coupling mode in Figs. 24(a) and (b).

The comparison of the detected outputs by the two outputs operating in the sample-and-hold mode is illustrated in Fig. 25. In Fig. 26 the output is shown as the difference of Output A minus Output B when input is applied only to Register A. Note that very good common mode rejection can be obtained.

The voltage gain of the output amplifier is defined as the ratio of the change of output voltage,  $\Delta V_{out}$ , (of Output A or Output B) to the change of the floating diffusion voltage,  $\Delta V_{FD}$ . The value of  $\Delta V_{out} / \Delta V_{FD}$  was measured to be 0.55. This was done by observing the change of the output voltage, Output A or Output B, due to a change of the drain voltage  $D_1$ .

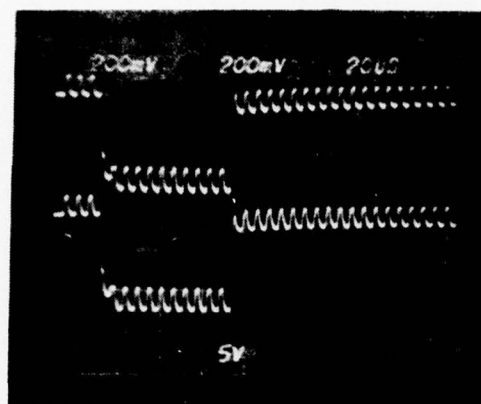


(a)

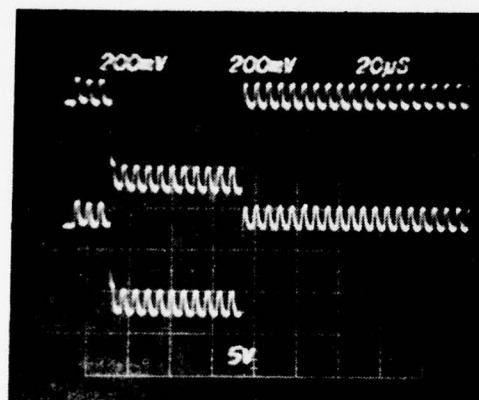


(b)

Figure 24. Output waveforms at 300 K for direct-coupling mode in (a) and for sample-and-hold mode in (b). The top trace in each photomicrograph is the Output A (200 mV/div). The lower trace is the applied input (5 V/div).



(a)



(b)

Figure 25. Waveforms for sample-and-hold mode at 300 K for Output A (top traces) and Output B (bottom trace) for operation without fat zero in (a), and with 10% fat zero in (b).

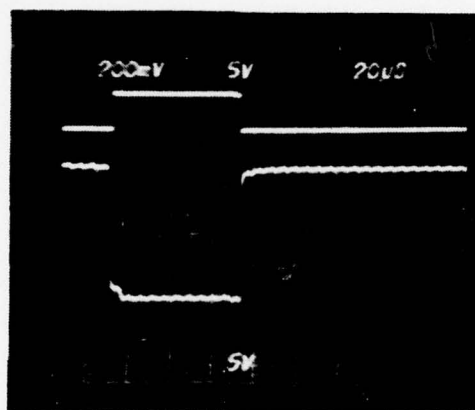


Figure 26. Input and output waveforms at 300 K without fat zero. The input is applied only to Register A, and the output is detected as the difference of A-B in the sample-and-hold mode.

The value of the total capacitance of the floating diffusion,  $C_{FD}$ , was estimated from the device geometry to be 0.19 pF. This value represents the sum of the following components:

- (1) Depletion capacitance of the floating diffusion for  
 $0.7 \times 1.2 \text{ mil} \times 0.04 \text{ pF/mil}^2 = \dots\dots\dots 0.03 \text{ pF}$
  - (2) Overlap capacitance of the floating diffusion by  
 gates  $G_4$  and gate R with channel oxide of  $1400 \text{ \AA}$   
 corresponding to capacitance of about  $0.14 \text{ pF/mil}^2$   
 is  $(2)(0.7)(0.15)(0.14) = \dots\dots\dots 0.03 \text{ pF}$
  - (3) The metal connection from the floating diffusion to  
 the first polysilicon gate of transistor  $Q_3$  or  $Q_4$  has  
 an area of  $0.45 \text{ mil}^2$  and oxide thickness of about  
 $3000 \text{ \AA}$  corresponding to capacitance of  $0.066 \text{ pF/mil}^2$   
 or total capacitance of  $(0.45)(0.066) = \dots\dots\dots 0.03 \text{ pF}$
  - (4) The first polysilicon gate has as two components of  
 capacitance:
    - (a) The gate over the  $p^+$  channel stops has an  
 area of  $0.9 \times 0.6 = 0.54 \text{ mil}^2$  at capacitance  
 of  $0.066 \text{ pF/mil}^2$  or total capacitance of  
 $(0.54)(0.066) = \dots\dots\dots 0.04 \text{ pF}$
    - (b) The source follower capacitance has an  
 effective area of  $1.4 \times 0.84 \text{ mil}^2$  with an  
 estimated capacitance of  $(0.5)(0.14) \text{ pF/mil}^2$ .  
 Thus, the capacitance of the source follower  
 channel is  $(0.84)(0.5)(0.14) = \dots\dots\dots 0.06 \text{ pF}$
- $\underline{\hspace{1.5cm}} \quad 0.19 \text{ pF}$
- Total calculated value of  $C_{FD} =$

The value of the floating-diffusion capacitance was also measured as the ratio of the charge signal to the change in the voltage of the floating diffusion. We have found that for the output register operating with a period of  $140 \text{ }\mu\text{s}$ , a current of  $0.9 \text{ nA}$  measured in the drain D1 corresponded to a  $400\text{-mV}$  change in the output voltage. For the above data we calculate a signal charge,  $Q$ , of  $0.126 \text{ pC}$  corresponding to a change of the floating diffusion voltage of  $727 \text{ mV}$ . Therefore, the measured value of the total floating diffusion capacitance was  $C_{FD} = Q/\Delta V_{FD} = 0.17 \text{ pF}$ .

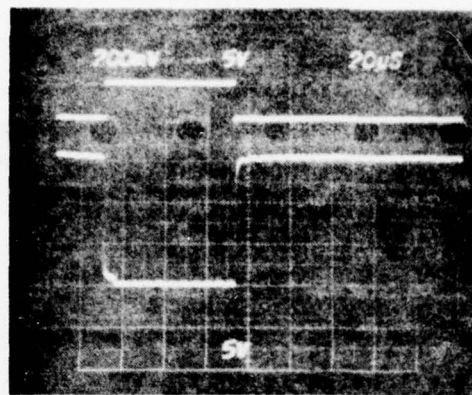
## 5. Transfer Losses of the Output Registers

The transfer loss measurements at 300 K are illustrated in Fig. 27. As is indicated by the output waveform in Fig. 27(a), the charge-transfer loss per transfer for operation without fat zero is about  $1.3 \times 10^{-4}$ . Application of 10% fat zero in Fig. 27(b) results in a decrease of the transfer-loss to about  $1.0 \times 10^{-4}$ . However, as shown in Fig. 27(c), operation with 10% fat zero and a reduced signal level to about 350 mV results in a transfer loss in the range of  $10^{-5}$ . The improvement of charge-transfer efficiency in Fig. 27(c) at lower signal level results from the fact that with larger charge signal, the buried channel becomes filled and the excess charge signal starts forming a surface channel. Similar results were observed at 77 K, in which case the charge-transfer losses were also found to be larger.

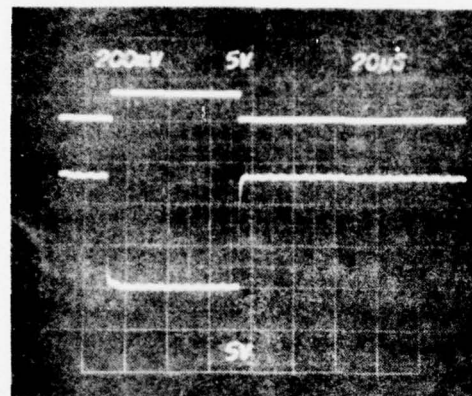
The charge-transfer losses at 77 K, however, in the tested devices operated without fat zero were found to depend on the dc bias voltage applied to gate  $G_4$  which is adjacent to the floating diffusions. The waveforms in Figs. 28 to 30 illustrate this observation. The charge-transfer losses at 77 K for operation without fat zero are about  $3 \times 10^{-4}$ ,  $1.6 \times 10^{-3}$ , and  $2 \times 10^{-4}$  for dc bias voltages on gate  $G_4$  of 0 V, 1.82 V, and 4 V, respectively. The bias voltage  $V_{G_4} = 1.82$  V corresponds to the maximum charge trapping loss observed, while the bias voltage  $V_{G_4} = 4$  V represents the maximum voltage before the detected output starts to become attenuated. This means that for  $V_{G_4}$  larger than 4 V the effective floating diffusion capacitance starts to increase.

Charge-transfer losses at 77 K for operation with about 10% fat zero were found to be about  $5 \times 10^{-5}$  and independent of the dc bias voltage applied to  $G_4$ .

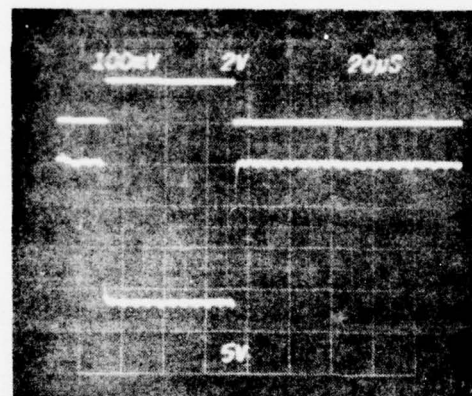
The effect of increasing the charge signal to the point where the excess charge starts forming a surface channel is illustrated in the comparison of the detected outputs in Fig. 30(b) and (c). While the charge-transfer loss is about  $5 \times 10^{-5}$  for an output signal of 300 mV, the increase of the signal level to 670 mV results in an increase of the transfer loss to  $1.3 \times 10^{-4}$ . The transition from the buried-channel operation to the mixed buried- and surface-channel operation was observed at an output signal level of about 350 mV. For floating diffusion capacitance  $C_{FD} = 0.19$  pF and output amplifier voltage gain of 0.55, this corresponds to a charge packet of 1.2 pC or  $7.5 \times 10^6$  electrons.



(a)

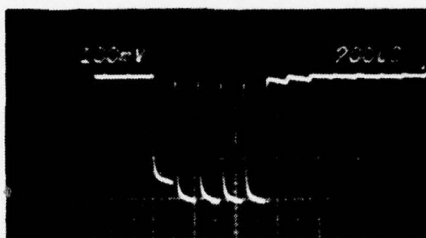


(b)

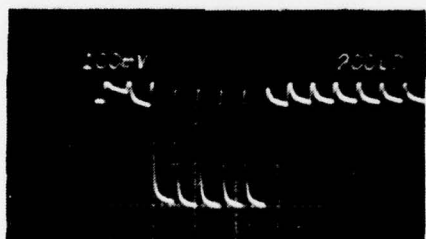


(c)

Figure 27. Input and output waveforms at 300 K for operation without fat zero in (a); with 10% fat zero in (b); and with 10% fat zero and reduced signal level in (c). Top trace in each photograph is the input A at 5 V/div in (a) and (b), and 2 V/div in (c). The lower trace in each photograph is the output A-B at 200 mV/div in (a) and (b), and 100 mV/div in (c).

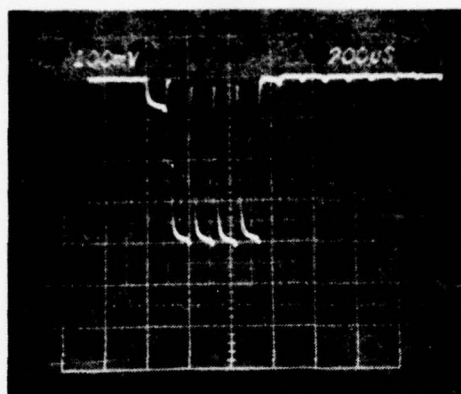


(a)

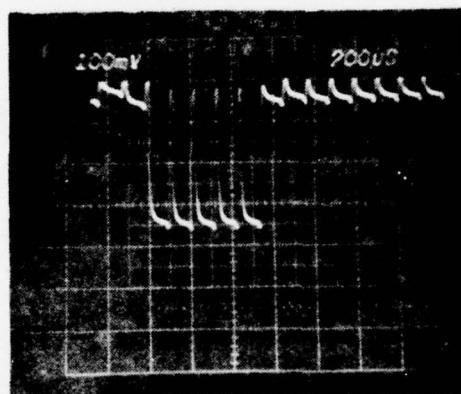


(b)

Figure 28. Output waveforms for a pulse input at 77 K,  $V_{G4} = 0$  V, and operation without fat zero in (a), and about 10% fat zero in (b).



(a)

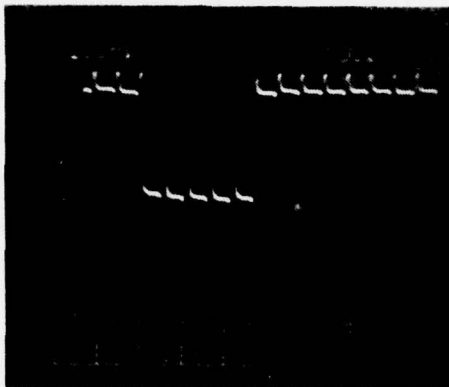


(b)

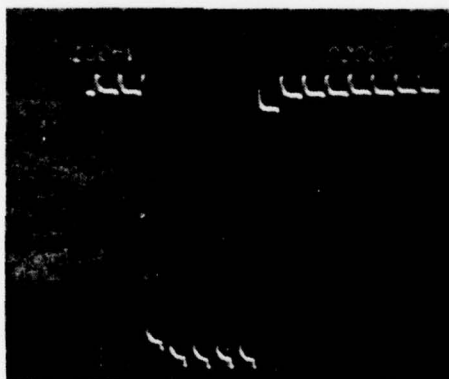
Figure 29. Output waveforms for a pulse input at 77 K,  $V_{G4} = 1.82$  V, and operation without fat zero in (a), and with about 10% fat zero in (b).



(a)



(b)



(c)

Figure 30. Output waveforms for a pulse input at 77 K,  $V_{G4} = 4$  V, and for operation without fat zero in (a); with about 10% fat zero in (b); and for an increased signal level with about 5% fat zero in (c).

## B. PRELIMINARY THERMAL IMAGING MEASUREMENTS

The thermal imaging with the 256-element IR-CCD line sensor was demonstrated at RADC/ET, Hanscom AFB, Massachusetts 01731, with R. W. Taylor and W. Ewing. For this test the device was cooled to about 80 K by an Air Products Displex Refrigerator with a sapphire entrance window. The thermal images were focused on the sensor arrays with  $f/1.2$  optics. The detected response of thermal images for 35 ms integration time is illustrated in Fig. 31. In (a) the skimming barrier gate  $G_{1T}$  is set to  $V_{G1T} = 2.06$  V and in (b) to  $V_{G1T} = 4.16$  V. The left part of each output is lower, as this section has been shielded by a low-temperature metal bracket. The pedestal in (a) and (b) represents the 300 K background, and the increased output signal on the right side corresponds to the image of a  $50^{\circ}\text{C}$  source. The increased sensitivity of the detectors from (a) to (b) implies a field enhanced reduction of the Schottky barriers.

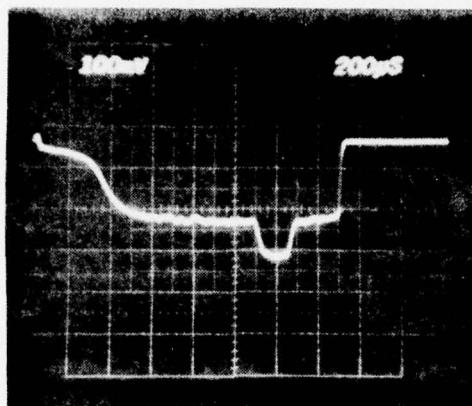
The two superimposed waveforms shown in Fig. 32 represent the "finger test," i.e., the thermal imaging of two human fingers that are about  $10^{\circ}\text{C}$  above the room-temperature background. This test illustrates that with  $f/1.2$  optics the IR-CCD imager has a responsivity of about 1.0 mV per  $^{\circ}\text{C}$ .

Inspection of the waveforms also shows that the random noise in the detected signal is on the order of 1.0 mV or less. Thus, the above test illustrates that the 256-element platinum silicide IR-CCD sensor is capable of a thermal resolution of less than  $1.0^{\circ}\text{C}$ . To achieve minimum noise in the output signal, the output amplifier was operated in the direct coupling mode. The sample-and-hold operation mode appeared to introduce an excess noise signal.

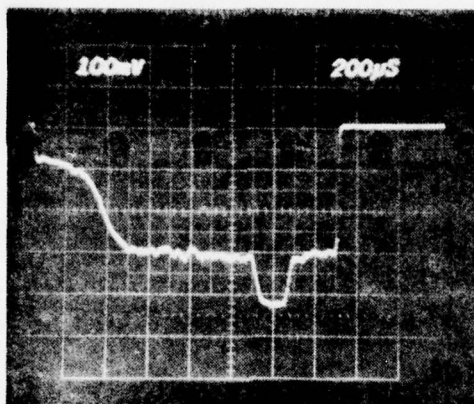
The best uniformity achieved with the 256-element IR-CCD arrays at RADC-ET was an 8.0% maximum peak-to-peak variation. This corresponds to about 1.2% rms uniformity from detector to detector. The thermal sensitivity measurements performed on two devices indicate a quantum efficiency coefficient  $C_1$  [1,2] of about 10% for the platinum silicide Schottky-barrier detectors.

## C. DISCUSSION OF RESULTS

The devices fabricated under this contract were studied at RCA Laboratories only at 300 K. The 77 K data presented in this report represents the initial evaluation of these devices at RADC/ET in collaboration with R. W. Taylor and



(a)



(b)

Figure 31. Thermal imaging waveforms at 300 K background and a 50°C slit with the 256-element IR-CCD operating at 80 K for dc bias voltage on GIT of 2.06 V in (a); and 4.16 V in (b). The optical integration time was 35 ms. The output is 100 mV/div.

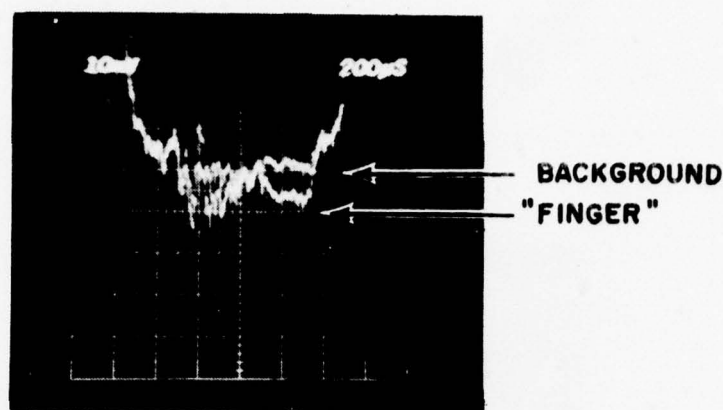


Figure 32. Two superimposed waveforms are detected thermal images of two human fingers at 10 mV/div.

W. Ewing. A more complete evaluation of the 256-element IR-CCD line sensors at low temperature will be done by RADC/ET.

The data on operation at 77 K with about 10% bias charge (fat zero) indicated a charge transfer loss of  $5 \times 10^{-5}$  per transfer. These results point out that the charge transfer loss is not a limiting factor for thermal imaging applications of platinum silicide Schottky-barrier IR-CCDs. This is because, in addition to the large thermal background signal normally present, a bias charge can also be introduced to preset the CCD output register to the low-loss state.

A somewhat anomalous behavior was observed for operation without fat zero at 77 K with the trapping-type transfer loss ranging from  $2 \times 10^{-4}$  to  $1.3 \times 10^{-3}$  as a function of the voltage applied to the dc-biased gate  $G_4$ . Therefore, more transfer loss measurements at 77 K are needed to explain these results.

The data at 77 K showed that the continuous-charge-skimming mode can result in a very low and uniform leakage current by allowing the platinum silicide Schottky-barrier devices to be operated at an arbitrary low reverse-bias voltage. The observed variation from unit to unit of the Schottky-diode leakage current can be explained as resulting from small mask misalignments between the implanted n-type guard rings and the contact opening defining the platinum silicide areas. Further work on improving the leakage current characteristics may be important for applications where it is advantageous to operate these devices at somewhat higher temperature than 77 K.

However, the most critical device parameter requiring more development is the uniformity of response from detector to detector. The observed maximum variation of response of 8.0% peak-to-peak, corresponding to about 1.2% rms variation, is still too large, and it should be possible to reduce it appreciably by designing the detectors in a more nearly square format, by reducing photolithographic defects, and by other processing improvements.

## SECTION V

### CONCLUSIONS

The development of the 256-element IR-CCD line sensor demonstrated that platinum-silicide Schottky-barrier detectors, useful for thermal imaging, can be fabricated together with double-polysilicon-gate buried-channel CCDs having good charge-transfer characteristics at 77 K.

The platinum silicide Schottky-barrier detectors were operated at 77 K with a leakage current density of  $1.4 \times 10^{-9}$  A/cm<sup>2</sup>, which allows sensor operation with optical integration time in excess of 100 ms.

Operation of the Schottky-barrier detectors in the continuous-charge-skimming mode was demonstrated. This detection mode allows the platinum silicide detectors to operate at an arbitrarily low reverse-bias voltage, thus producing very low and very uniform leakage current density. To minimize the leakage current at 77 K, the platinum silicide Schottky-barrier detectors were also fabricated with implanted n-type diffusion guard rings.

The developmental platinum silicide Schottky-barrier infrared detectors have quantum efficiency coefficient  $C_1$  [1,2] of about 0.1 and response uniformity variation of about 8.0% maximum peak-to-peak, or about 1.2% rms. The preliminary thermal imaging data indicates that the developed IR-CCD line sensors are capable of thermal resolution of less than 1°C in a 300 K background. Better performance, however, is expected with more work on device processing and circuit techniques.

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# METRIC SYSTEM

## BASE UNITS:

Quantity	Unit	SI Symbol	Formula
length	metre	m	...
mass	kilogram	kg	...
time	second	s	...
electric current	ampere	A	...
thermodynamic temperature	kelvin	K	...
amount of substance	mole	mol	...
luminous intensity	candela	cd	...

## SUPPLEMENTARY UNITS:

plane angle	radian	rad	...
solid angle	steradian	sr	...

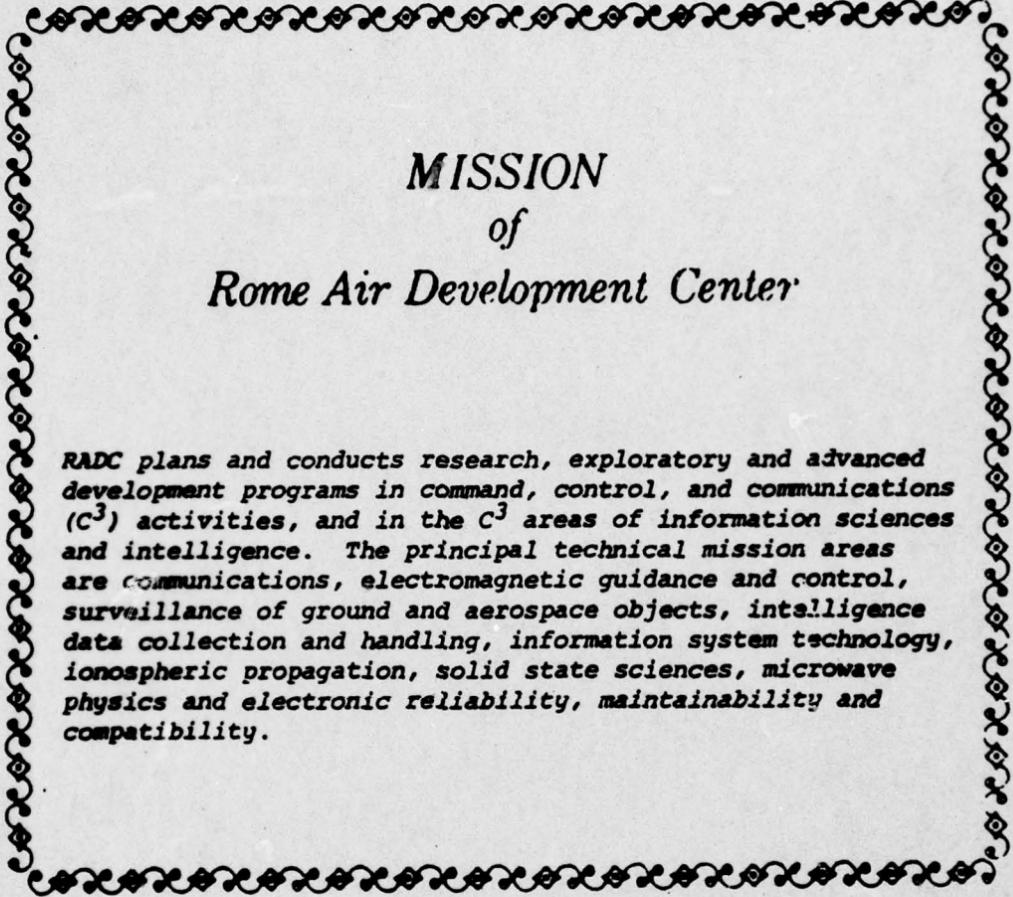
## DERIVED UNITS:

Acceleration	metre per second squared	...	m/s
activity (of a radioactive source)	disintegration per second	...	(disintegration)/s
angular acceleration	radian per second squared	...	rad/s
angular velocity	radian per second	...	rad/s
area	square metre	...	m
density	kilogram per cubic metre	...	kg/m
electric capacitance	farad	F	A·s/V
electrical conductance	siemens	S	A/V
electric field strength	volt per metre	...	V/m
electric inductance	henry	H	V·s/A
electric potential difference	volt	V	W/A
electric resistance	ohm	...	V/A
electromotive force	volt	V	W/A
energy	joule	J	N·m
entropy	joule per kelvin	...	J/K
force	newton	N	kg·m/s
frequency	hertz	Hz	(cycle)/s
illuminance	lux	lx	lm/m
luminance	candela per square metre	...	cd/m
luminous flux	lumen	lm	cd·sr
magnetic field strength	ampere per metre	...	A/m
magnetic flux	weber	Wb	V·s
magnetic flux density	tesla	T	Wb/m
magnetomotive force	ampere	A	...
power	watt	W	J/s
pressure	pascal	Pa	N/m
quantity of electricity	coulomb	C	A·s
quantity of heat	joule	J	N·m
radiant intensity	watt per steradian	...	W/sr
specific heat	joule per kilogram-kelvin	...	J/kg·K
stress	pascal	Pa	N/m
thermal conductivity	watt per metre-kelvin	...	W/m·K
velocity	metre per second	...	m/s
viscosity, dynamic	pascal-second	...	Pa·s
viscosity, kinematic	square metre per second	...	m/s
voltage	volt	V	W/A
volume	cubic metre	...	m
wavenumber	reciprocal metre	...	(wave)/m
work	joule	J	N·m

## SI PREFIXES:

Multiplication Factors	Prefix	SI Symbol
1 000 000 000 000 = 10 <sup>12</sup>	tera	T
1 000 000 000 = 10 <sup>9</sup>	giga	G
1 000 000 = 10 <sup>6</sup>	mega	M
1 000 = 10 <sup>3</sup>	kilo	k
100 = 10 <sup>2</sup>	hecto*	h
10 = 10 <sup>1</sup>	deka*	da
0.1 = 10 <sup>-1</sup>	deci*	d
0.01 = 10 <sup>-2</sup>	centi*	c
0.001 = 10 <sup>-3</sup>	milli	m
0.000 001 = 10 <sup>-6</sup>	micro	μ
0.000 000 001 = 10 <sup>-9</sup>	nano	n
0.000 000 000 001 = 10 <sup>-12</sup>	pico	p
0.000 000 000 000 001 = 10 <sup>-15</sup>	femto	f
0.000 000 000 000 000 001 = 10 <sup>-18</sup>	atto	a

\* To be avoided where possible



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*RADC plans and conducts research, exploratory and advanced development programs in command, control, and communications (C<sup>3</sup>) activities, and in the C<sup>3</sup> areas of information sciences and intelligence. The principal technical mission areas are communications, electromagnetic guidance and control, surveillance of ground and aerospace objects, intelligence data collection and handling, information system technology, ionospheric propagation, solid state sciences, microwave physics and electronic reliability, maintainability and compatibility.*

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